AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-4 Lec-1

Avinash Sir

Today's target

- Logic families
- TTL NAND gate
- Noise margin, propagation delay, fan-in, fan-out, tristate TTL
- PYQ

Gateway Classes

AKTU : *DIGITAL SYSTEM DESIGN (BEC-302)* Syllabus

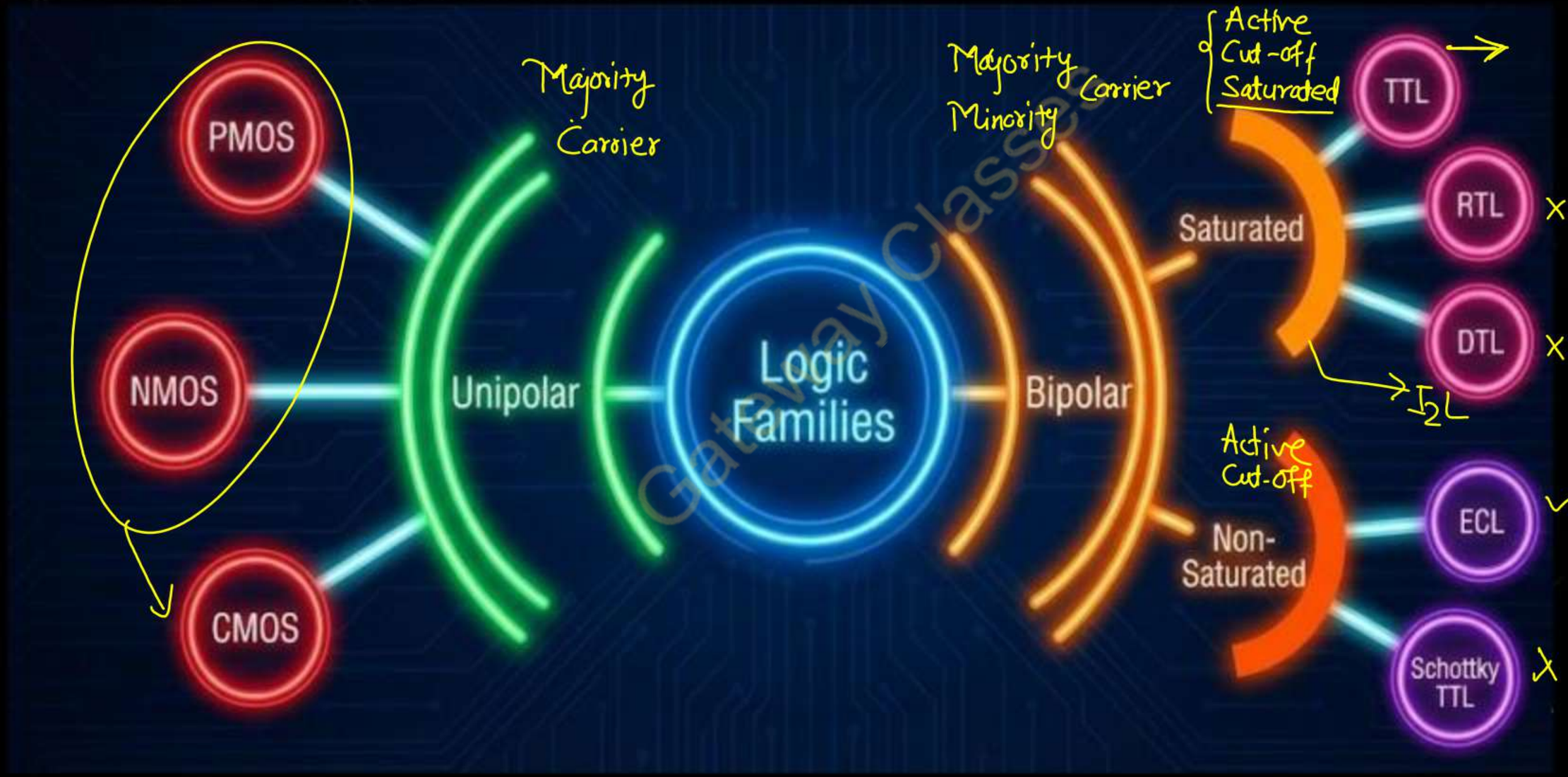
UNIT- 4

- Logic families and semiconductor memories: TTL NAND gate, specifications, noise margin, propagation delay, fan-in, fan-out, tristate TTL, ECL, CMOS families and their interfacing, memory elements, concept of programmable logic devices like FPGA, logic implementation using programmable devices.

Gateway Classes

Logic Families

it is a group of compatible ICs with the same logic levels and supply voltages fabricated for performing various logical functions.



Characteristics of a Logic Family

(speed of operation)

1. Propagation Delay This is the "reaction time" of the logic gate. It measures how fast a signal travels through the gate.

Definition: The time interval between the application of an input signal and the change in the output signal.

Measurement: It is measured in nanoseconds (n_s) or picoseconds (p_s).

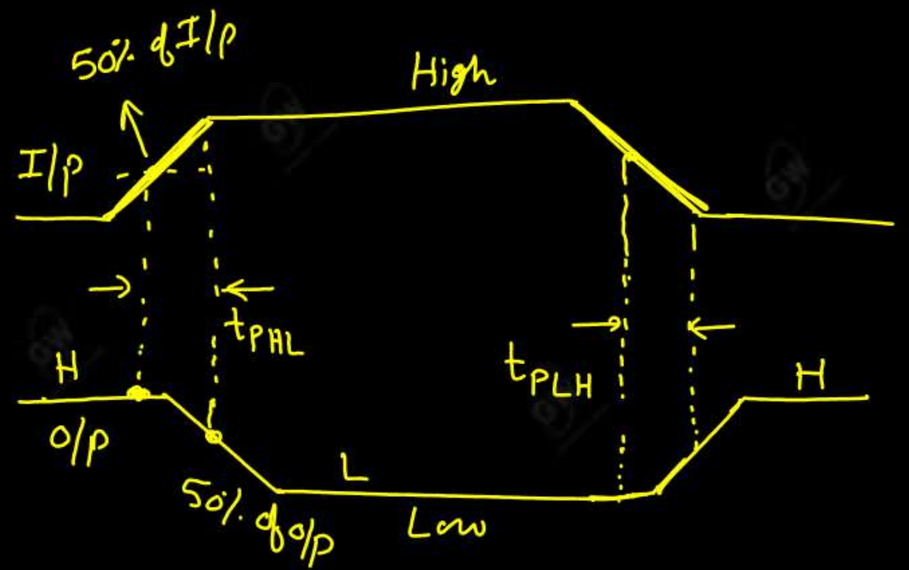
It is usually defined by two specific metrics:

t_{PHL} : Time taken for the output to switch from High to Low.

t_{PLH} : Time taken for the output to switch from Low to High.

Average Delay: $t_{pd} = (t_{PHL} + t_{PLH})/2$

Significance: This limits the maximum speed (frequency) at which a digital system can run. If the delay is too long, the next stage of the circuit won't receive the data in time.



Gateway Classes

Transistor-Transistor Logic (TTL) as NAND Gate Operation

Logic levels in TTL:

Logic 0 ≈ VCE(sat) ≈ 0.2 V

Logic 1 ≈ VCC = 5 V

For p–n junction (diode operation)

Voltage across a conducting diode ≈ 0.7 V

Cut-in (threshold) voltage ≈ 0.6 V

For Transistor

Base–Emitter voltage in saturation (V_{BE},sat) ≈ 0.8 V

Base–Emitter cut-in voltage (V_{BE}cut-in) ≈ 0.5 V

Collector–Emitter saturation voltage (V_{CE},sat) ≈ 0.2 V

Gateway Classes

Power dissipation :-

⇒ Power supply by V_{cc} . dissipate in form of heat

Power dissipation = $V_{cc} \cdot I_{cc}$

Power dissipation is generally in milli watt.

Figure of merit :-

= Power dissipation × Propagation delay.

Ex. F.O.M = 5mW × 20ns

= 100 P. Joule.

Gateway Classes

Characteristics of a Logic Family

2. Noise Margin (Immunity):- In the real world, signals are never perfect. "Noise" (unwanted electrical interference) often gets added to the signal as it travels through wires. The Noise Margin is the safety buffer that ensures a logic gate doesn't mistake a "High" signal for a "Low" one (or vice versa) due to this noise.

Definition: The maximum noise voltage that can be added to an input signal without causing an error in the output. Logic gates have a "legal" range for High and Low voltages.

V_{OH}: Minimum voltage a gate outputs for a HIGH.

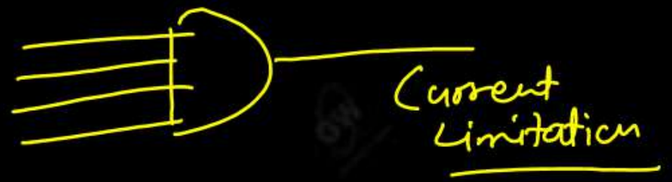
V_{IH}: Minimum voltage a gate accepts as a HIGH.

The difference V_{OH} - V_{IH} is the High-State Noise Margin (NM_H).

Similarly, the Low-State Noise Margin (NM_L) is the difference between what a gate accepts as Low (V_{IL}) and what the previous gate outputs as Low (V_{OL}).

Gateway Classes

Characteristics of a Logic Family



3. Fan-in : This is a physical limitation of the input side of the gate. The number of inputs that a single logic gate is designed to handle.

Example: A 2-input NAND gate has a fan-in of 2; an 8-input NAND gate has a fan-in of 8.

4. Fan-out This is the "muscle" or driving capability of the gate's output. The maximum number of standard inputs (loads) of the same logic family that a single logic gate output can drive reliably.

Current Limit (DC Fan-out): In families like TTL, the output transistor must sink or source current for every input it drives. If you connect too many inputs, the output voltage will drop (or rise) into the "forbidden" zone, causing errors.

Speed Limit (AC Fan-out): In families like CMOS, the inputs are capacitors. Adding more inputs adds more "capacitive load." The gate might still work, but it will take much longer to charge up all those capacitors, drastically increasing Propagation Delay.

Gateway Classes

Transistor-Transistor Logic (TTL)

The Transistor-Transistor Logic (TTL) is a logic family made up of BJTs (bipolar junction transistors. The best examples of TTL are logic gates namely the 7402 NOR Gate & the 7400 NAND gate.

It is a digital logic family that uses bipolar junction transistors (BJTs) for both Input switching & Output driving. Supply voltage is +5V DC.

In DTL, diodes are used in the input stage, which cause large delay due to diode storage time. TTL uses transistors instead of diodes, resulting in much faster switching.

It also offers Higher Noise Immunity, Better Fan-out Capability, Improved Temperature Stability

Gateway Classes

Transistor-Transistor Logic (TTL) as NAND Gate

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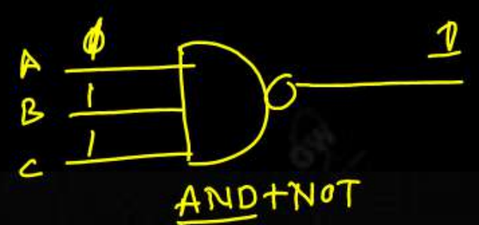
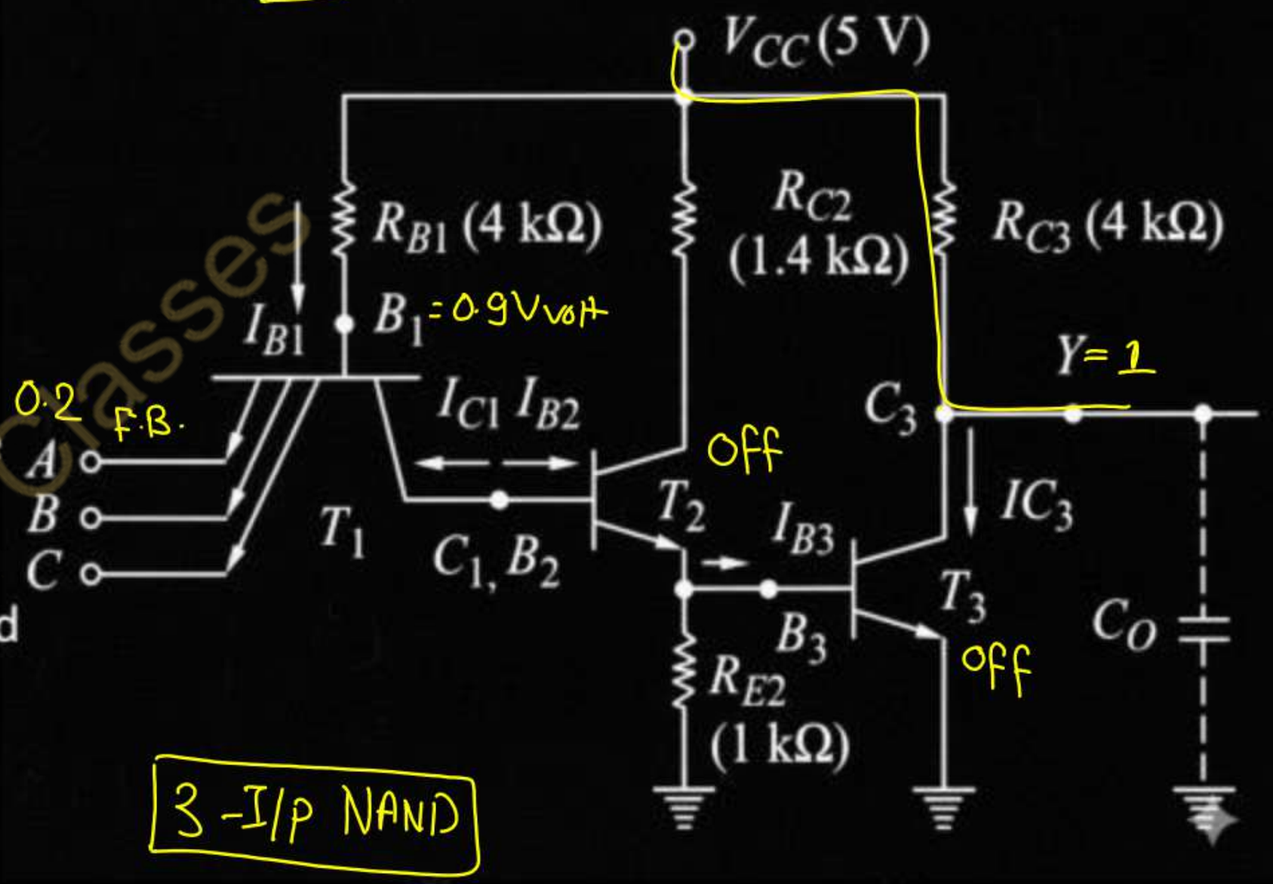
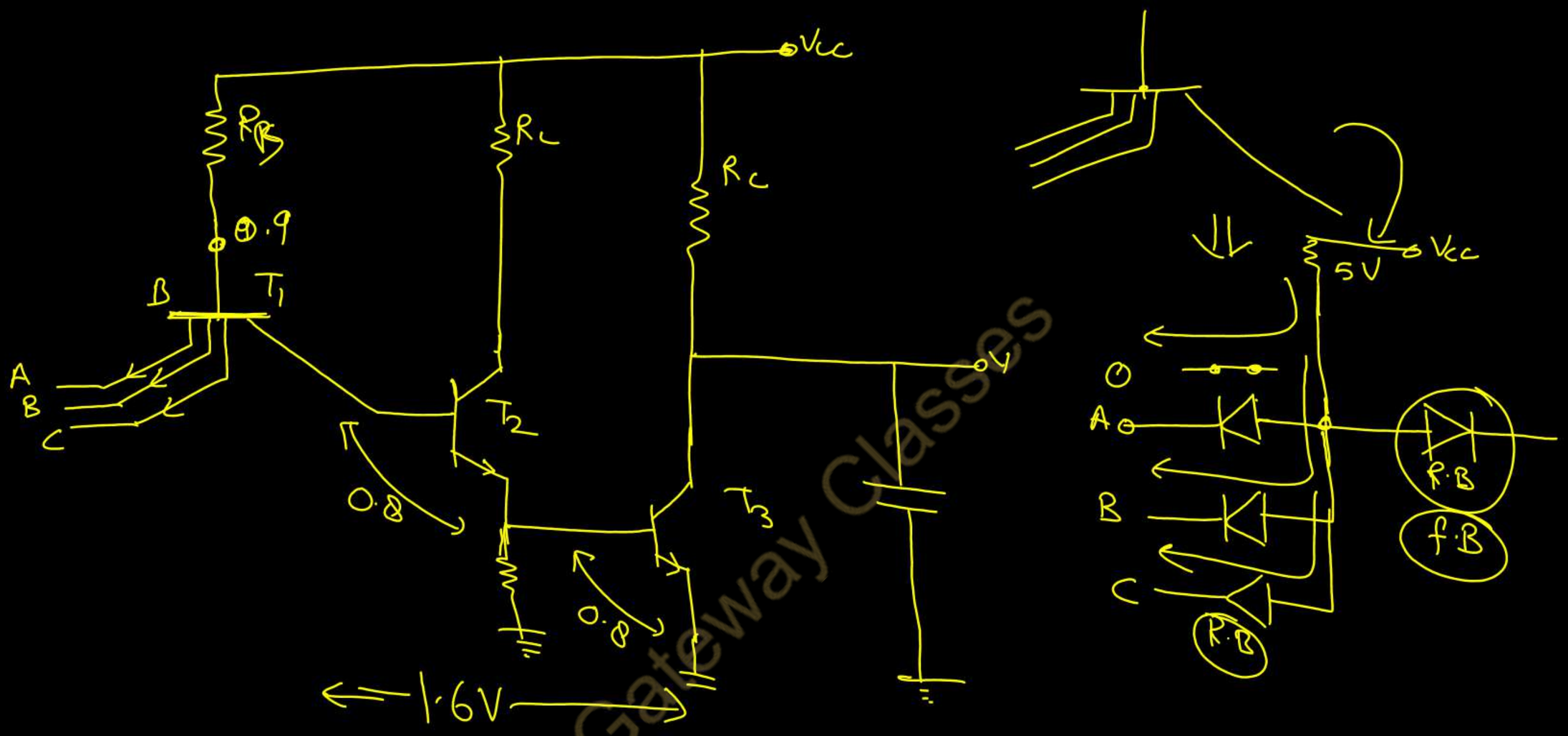


Operation :- For NAND Gate output is low when all inputs are high if any input is low output is always high.

- **Case-1 (When at least one input is low)**
- The emitter-base junction of transistor T1 becomes forward biased.
- T1 enters into forward active mode, establishing a base voltage of VB1 = 0.9V.
- For the base-collector junction of T1 to become forward biased—and for transistors T2 and T3 to conduct—the voltage VB1 is required to be at least 1.6V.
- Since the actual voltage is insufficient (0.9V is less than the required 1.6V), transistors T2 and T3 remain in cut-off. And the output (o/p) will be high.



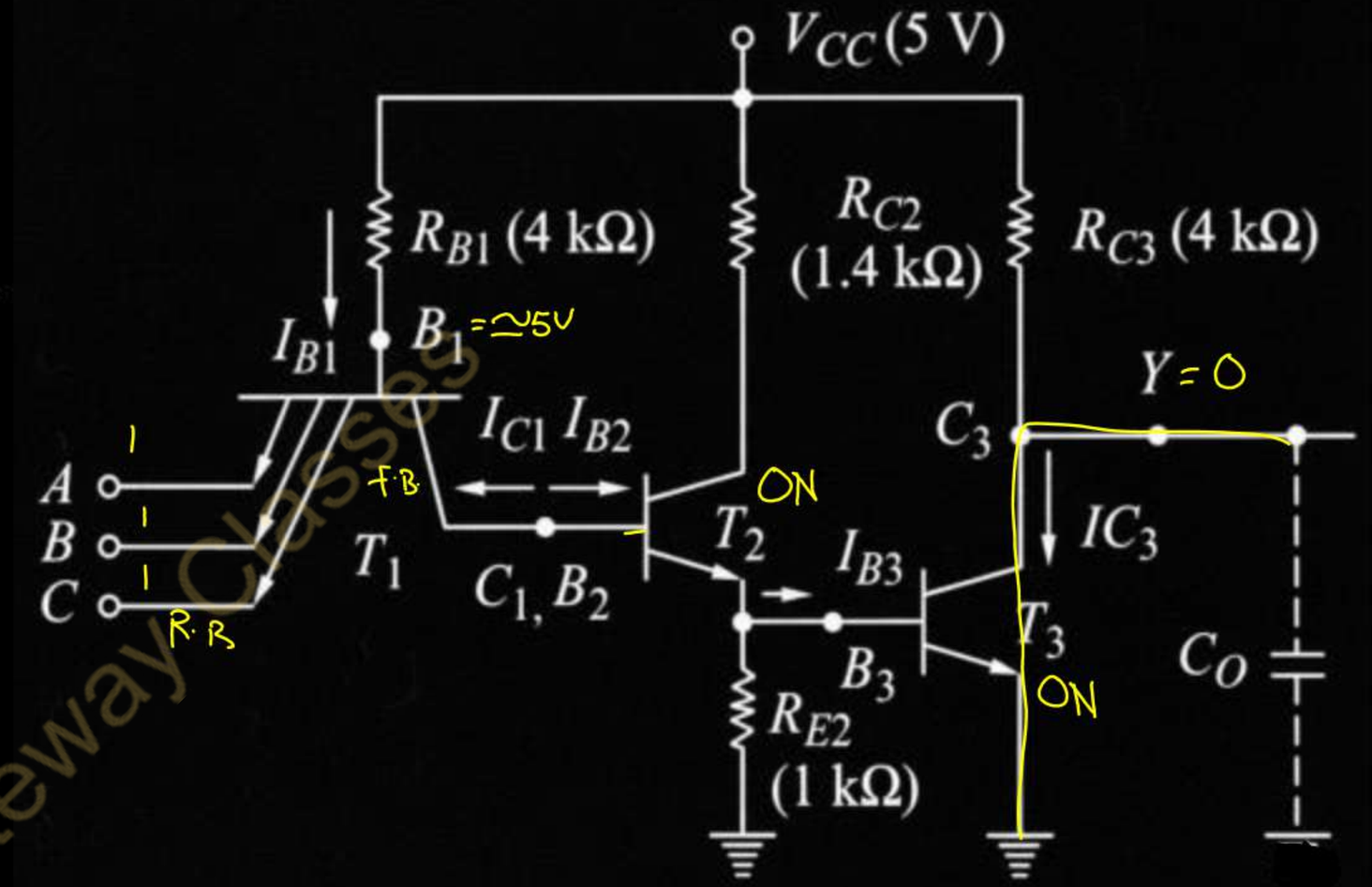
Gateway Classes



Gateway Classes

Case-2 (When all inputs are high)

- The emitter-base junction of transistor T1 becomes reversed biased.
- Point is connected to Vcc.
- Base current is supplied to drive the T2 & T3.
- T2 & T3 goes into saturation (ON)
- So out put will be equal to 0.2 volt (Low)
- So the NAND Gate Operation is verified.



Gateway Classes

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GATEWAY CLASSES

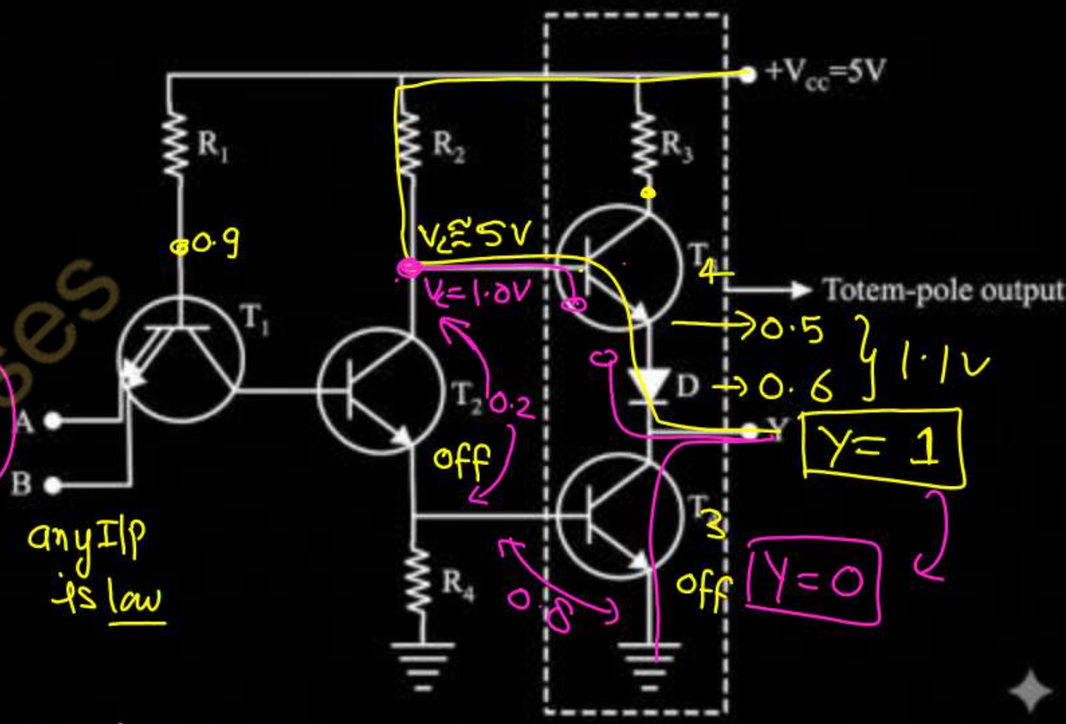
Output configuration of TTL

1. Totem-pole output
2. open collector output
3. Tri-state gate output

Gateway Classes

Totem-pole output

- Transistor T3, T4, diode D and current limiting resistor R3 form the totem-pole output configuration of TTL.
- There are a few advantages of using this configuration. When the output switches from LOW to a HIGH state, the output transistor T4 goes from saturation to cut off.
- During this transition, the load capacitance across T3 charges exponentially from low to a high voltage level.
- Due to the low output impedance of both transistors T3 and T4, the output voltage can change quickly from LOW to HIGH value as the capacitance charge and discharge quickly.



(i) If Any I/P is low
T_2 & T_3 = off, $V_c = V_{cc}$, T_4 & D Conduct, Y=1

(ii) If both I/P is high
T_2 & T_3 = ON, $V_c = 0.2 + 0.8 = 1V$, It is insufficient to conduct T_4 & D. hence o/p Y is connected to ground Y=0

Gateway Classes

Totem-Pole Output Advantages

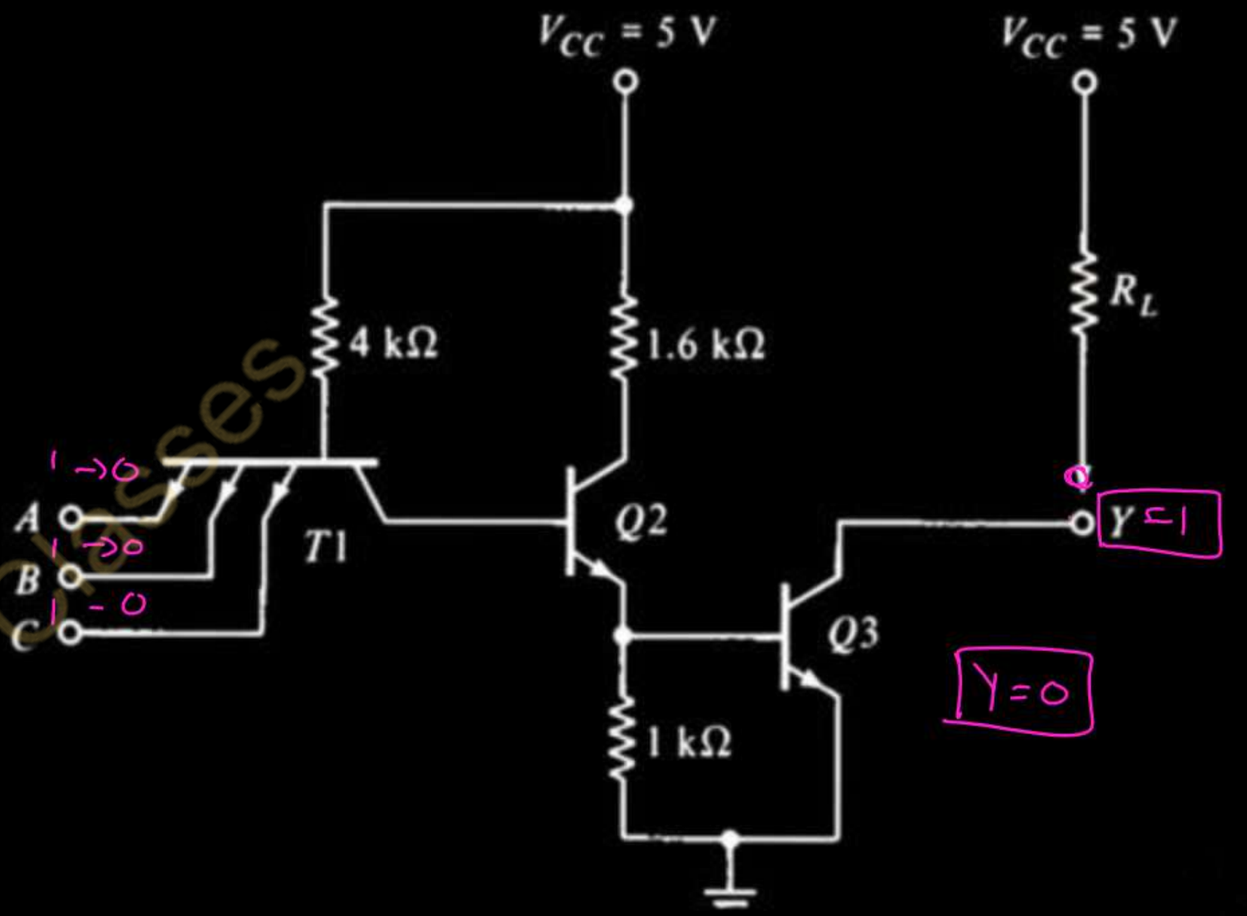
- ***High speed switching*** → Due to push-pull action (one transistor sources current while the other sinks), output changes state quickly.
- ***Low output impedance*** → Provides strong drive current to the next stage; minimizes propagation delay.
- ***Well-defined output voltage levels*** → Logic HIGH is close to Vcc and logic LOW close to ground.
- ***Less power dissipation at static states*** → Current flows only during switching moments.
- **Limitations**
- ***Cannot be wired-OR / wired-AND*** → Outputs must not be directly connected together; doing so may cause short-circuit between HIGH and LOW drivers.
- ***Noise spikes during switching*** → Due to cross-conduction (both transistors may momentarily conduct).
- ***Requires precise timing design*** → Shoot-through current must be controlled to avoid heating and damage.
- ***Not suitable for driving large loads*** → Limited current for external devices like relays, motors, lamps.

Gateway Classes

Open collector output

With any of the input at logic low, the corresponding emitter-base junction is forward biased and the voltage drop across the base of T1 is around 0.9V, not enough for the transistors T2 and T3 to conduct. Thus the output is either floating or Vcc, i.e. High level.

Similarly, when all inputs are high, all base-emitter junctions of T1 are reverse biased and transistor T2 and T3 get enough base current and are in saturation mode. The output is at logic low.



Gateway Classes

Open collector output

Advantages

- ***Supports wired-OR / wired-AND logic*** → Multiple outputs can be tied together using a pull-up resistor.
- ***Can interface with different voltage levels*** , Example: TTL 5V output can drive 12V logic using pull-up.
- ***Ideal for driving high-power loads*** → Relays, motors, LEDs can be driven using an external power supply.
- ***Easy to use in bus systems and multi-source signaling*** → One line shared by many drivers.

Limitations

- ***Slower switching*** → Rising edge is slow because output goes HIGH through pull-up resistor (passive pull-up).
- ***Higher power consumption*** → Pull-up resistor continuously draws current when output is LOW.
- ***Output HIGH level depends on pull-up value and load*** → Might not be ideal for fast / high-fan-out logic.
- ***Extra components required*** → A pull-up resistor must be added externally.

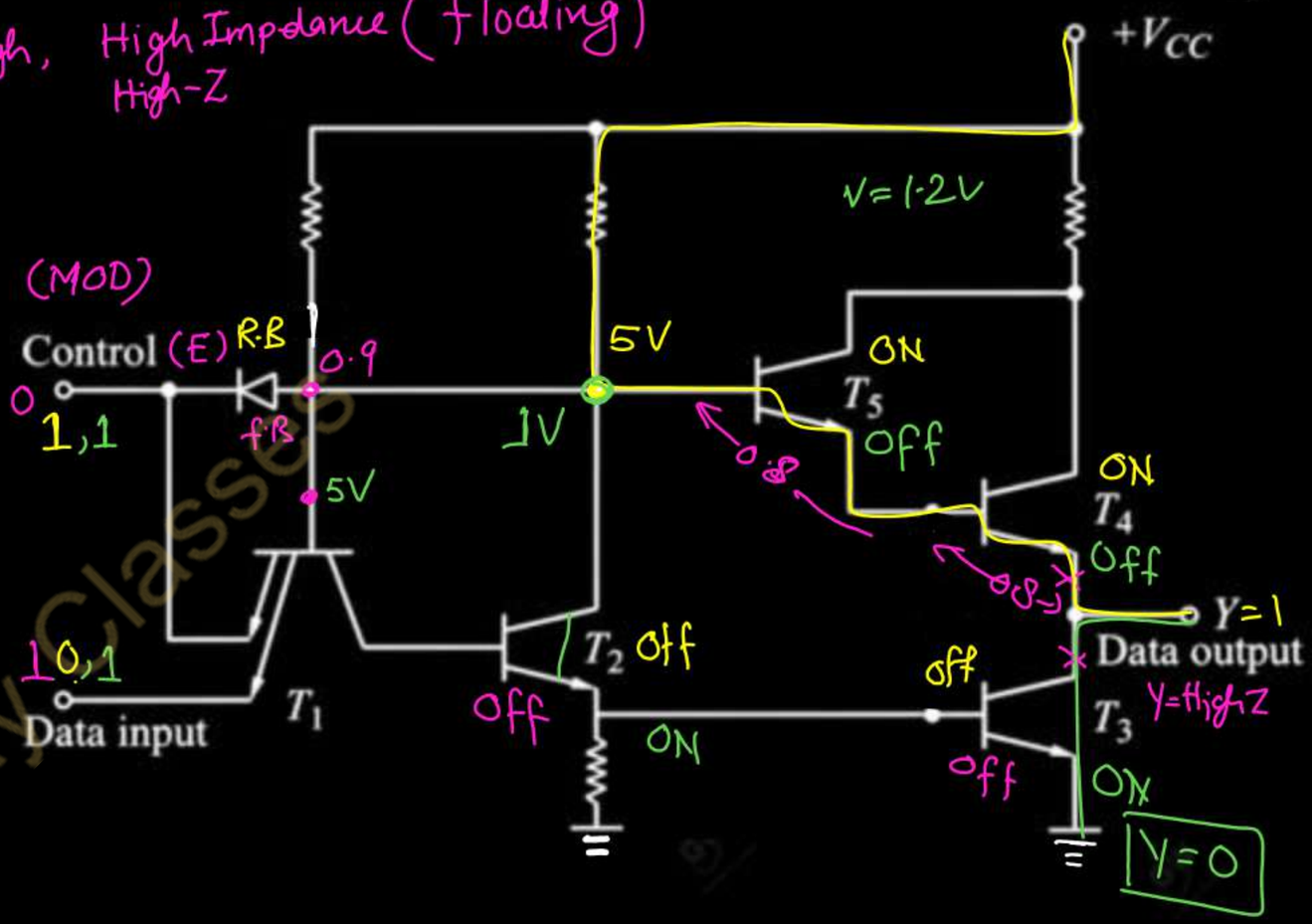
Gateway Classes

3. Tri-state gate output

Y = 0, 1
Low, high, High Impedance (floating)
High-Z

This configuration allows the output to effectively "disconnect" from the circuit, acting like an open switch. This is essential for computers where many devices share a single data wire (a Bus).

A tri-state output combines the benefits of both totem-pole output and open-collector output. Three states can be seen for the circuit with Tri-state output.

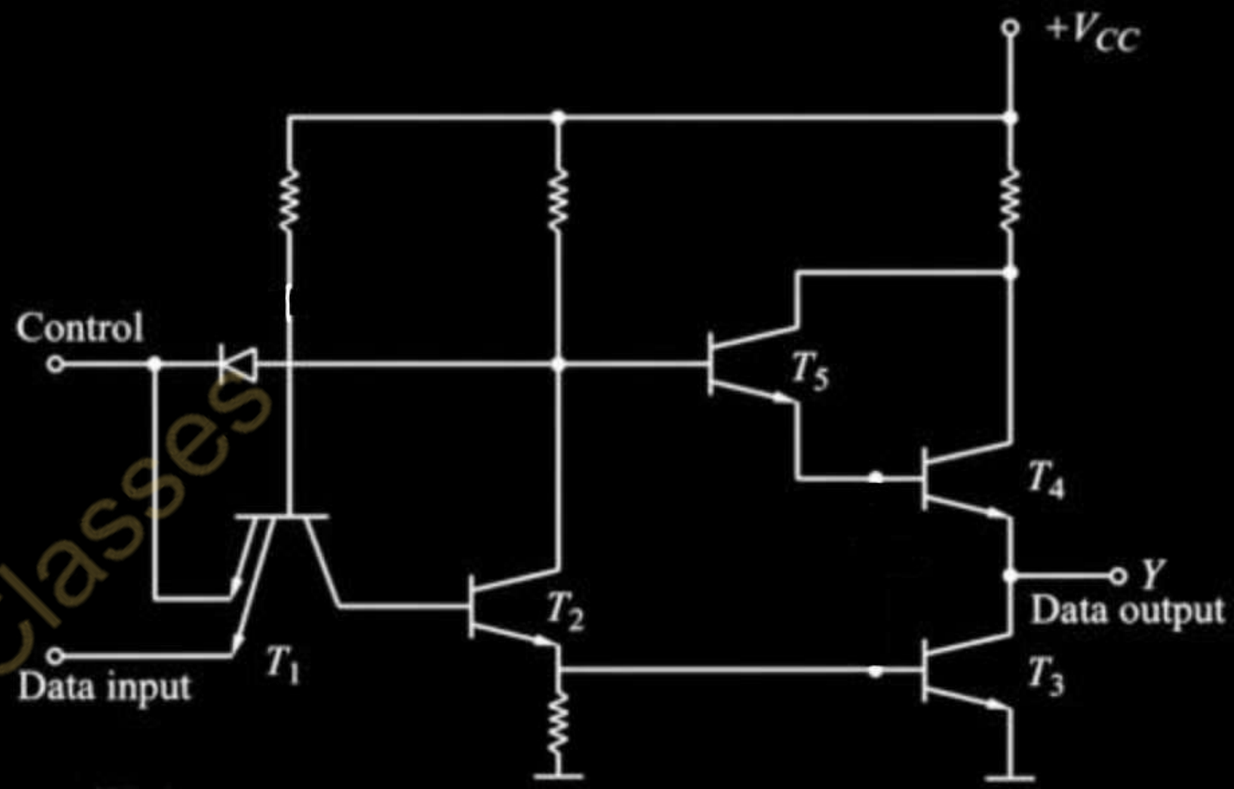


- Such circuits have an extra control input. If the control input is 1 the normal NAND operation is seen.
- When control input is 1 and all inputs are high, ***logic 0*** is seen.
- When control input is 1 and one of the inputs or all the inputs are 0, ***logic 1*** is seen.
- A ***high impedance*** also called the open-circuit state is seen when the control input is 0. In this case, the circuit behaves as if the output is disabled.

Gateway Classes

3. Tri-state gate output

- When control state C is HIGH and any input is LOW: Transistor T1 is ON, transistors T2 and T3 are OFF and transistors T4 and T5 are ON. The output is at a HIGH level.
- When control state C is HIGH and both inputs are HIGH: Transistor T1 is OFF, transistors T2 and T3 are ON and transistors T4 and T5 are OFF. The output is at a LOW level.



Gateway Classes

- When control state C is LOW: Irrespective of any input, transistor 1 is ON and all other transistors are OFF. The circuit is at HIGH impedance state.
- When control input is HIGH the circuit behaves similar to the totem-pole output circuit.
- When control input is LOW the circuit output is open-circuited.

3. Tri-state gate output (INVERTER)

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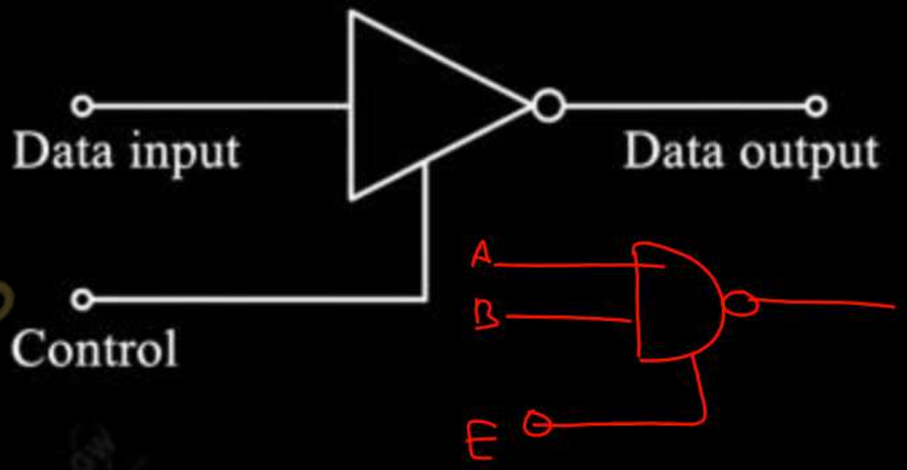
- With E = 1, the circuit operates as a normal INVERTER because the high input at E has no effect on transistor Q1 or diode D2. In this enabled condition the output is simply the inverse of logic input



DATA INPUT	CONTROL INPUT(E)	OUTPUT
0	0	HIGH- Z
1	0	HIGH-Z
0	1	1
1	1	0

Gateway Classes

Advantages of Tri-State Gate Output

- Allows multiple devices to share a common bus.
- Eliminates short-circuit conflicts between logic drivers
- Enables bus-oriented system design
- Provides better expandability
- Reduces wiring complexity
- Improves system reliability and performance
- Supports controlled access using enable signal

Gateway Classes

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GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-4 Lec-2

Today's target

- ECL Logic families
- CMOS
- PYQ

Gateway Classes

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AKTU : ***DIGITAL SYSTEM DESIGN (BEC-302)*** **Syllabus**

UNIT- 4

- Logic families and semiconductor memories: TTL NAND gate, specifications, noise margin, propagation delay, fan-in, fan-out, tristate TTL, ECL, CMOS families and their interfacing, memory elements, concept of programmable logic devices like FPGA, logic implementation using programmable devices.

Gateway Classes

ECL Logic Families
(unsaturated)

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- The TTL family uses transistors operating in the saturation mode. As a result, their switching speed is limited by the storage delay time associated with a transistor that is driven into saturation.

- Another logic family has been developed that prevents transistor saturation, thereby increasing *overall switching speed* by using a radically different circuits structure, called Current Mode Logic (CML). This logic family is also called Emitter-Coupled Logic (ECL).

CML

- Unlike TTL and CMOS families, ECL does not produce a large voltage swing between the LOW and HIGH levels. It has a small voltage swing, less than a volt, and it internally switches current between two possible paths, depending on the output state.

Gateway Classes

Characteristics of a ECL Logic Family

1. **Highest Speed Logic Family :-** ECL is the fastest among all logic families. 10K and 100K ECL have propagation delays around 1 ns. Newer versions like ECL-in-PS achieve delays below 0.5 ns (500 ps).

2. **No Transistor Saturation:-** Transistors are deliberately prevented from entering complete saturation, which avoids storage delays and allows very fast switching.

3. **Small Logic Level Swing:-** The voltage difference between logic HIGH and LOW is kept very small. This prevents transistors from saturating when the input goes from LOW to HIGH.

4. **Low Noise Margins**:- Because the logic levels are close together, ECL has poor noise immunity and is more sensitive to noise compared to other logic families.

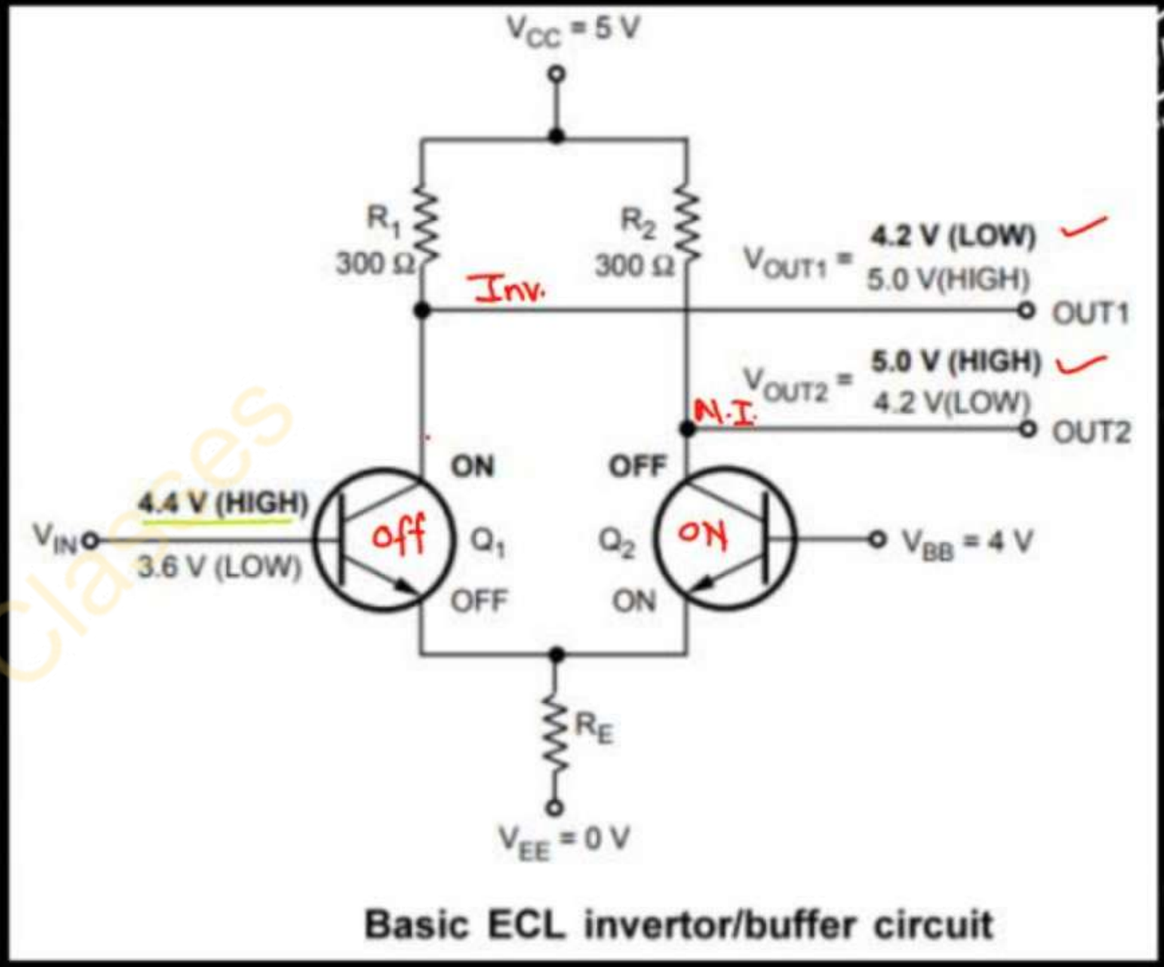
5. **High Power Consumption**:- Since transistors continuously operate in the active region (not saturated), ECL circuits consume more power.

6. **Low Switching Transients:-** The power supply current in ECL remains almost constant, resulting in lower switching noise than TTL or CMOS circuits.

Gateway Classes

Basic ECL Circuit

- It consists of two transistors connected in differential single ended input mode with a common emitter resistance. The circuit has two outputs : inverting output (OUT1) and noninverting output (OUT2). For this circuit, the input LOW and HIGH voltage levels are defined as 3.6 V and 4.4 V, and it produces output LOW and HIGH levels as 4.2 V and 5.0 V.



Basic ECL invertor/buffer circuit

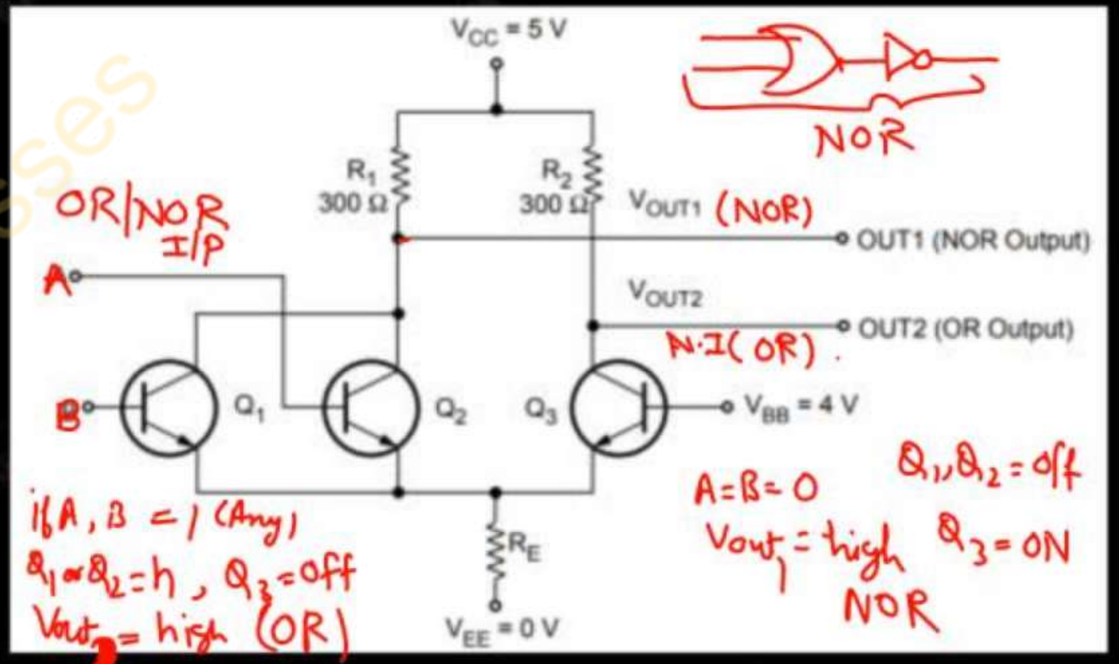
- When V_{IN} is HIGH (4.4 V), (see bold figures) transistor Q_1 is ON, but not saturated and transistor Q_2 is OFF. Thus, V_{OUT2} is pulled to 5.0 V (HIGH) through R_1 and drop across R_2 is 0.8 V so that V_{OUT2} is 4.2 V (LOW).
- When V_{IN} is LOW (3.6 V) (see normal figures), transistor Q_2 is ON, but not saturated and transistor Q1 is OFF. Thus, V_{QUT1} is pulled to 5.0 V (HIGH) through R_1 and drop across R2 is 0.8 V so that V_{OUT2} is 4.2 V (LOW).

Gateway Classes

2-Input ECL OR / NOR Gate

There has an additional transistor in parallel with Q1 as compared to ECL inverter. When the inputs applied at both the Q1 & Q2 transistors are low then will make the output1 (Vout1) to a HIGH value. So, this Vout1corresponds to the output of the NOR gate.

- Simultaneously, if the Q3 transistor is turned ON, then it will make the second output (Vout2) to be HIGH. So, this Vou2 output corresponds to the OR gate output.
- In the same way, if both the Q1 &Q2 transistors inputs are HIGH, then it will turn on the Q1 & Q2 transistors and provides the low output at the VOUT1 terminal.
- If the Q3 transistor is turned OFF throughout this operation then it will provide high output at the VOUT2 terminal.



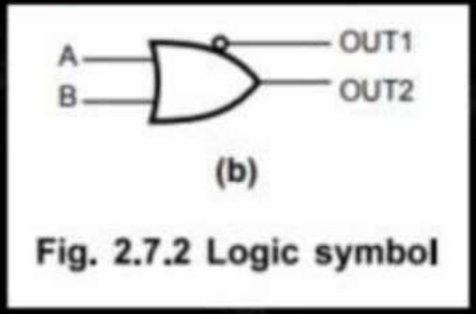


Fig. 2.7.2 Logic symbol

Gateway Classes

Advantages and Disadvantages of ECL Family

Advantages of ECL family

1. It is a fastest logic family. Offers propagation delay about 1 ns.
2. Transistors are not allowed to go into complete saturation and thus eliminating storage delays.
3. Less switching transients since power supply current is more stable.
4. Large fan-out.

Disadvantages of ECL family

1. Low noise immunity.
2. High power dissipation.

Gateway Classes

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GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-4 Lec-3

Gateway Classes

Today's target

- CMOS Logic families
- PYQ

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AKTU : ***DIGITAL SYSTEM DESIGN (BEC-302)*** **Syllabus**

UNIT- 4

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Gateway Classes

MOS Families

Digital circuits with MOSFETs can be grouped into three categories :

- PMOS – uses only P-channel enhancement MOSFETs,
- NMOS - uses only N-channel enhancement MOSFETs, and
- CMOS (complementary MOS) - uses both P and N-channel devices.

Gateway Classes

CMOS Inverter

AKTU 2024-25,23-24,22-23,21-22

It consists of two MOSFETs in series in such a way that the p-channel device has its source connected to + VDD (a positive voltage) and the n-channel device has its source connected to ground. The gates of the two devices are connected together as the common input and the drains are connected together as the common output.

1. When input is HIGH, the gate of Q_2 (p-channel) is at 0 V relative to the source of Q1 i.e. $V_{gS1} = 0$ V. Thus, Q_1 is OFF. On the other hand, the gate of Q_2 (n-channel) is at +VDD relative to its source i.e. V_{gS2} = +VDD. Thus, Q_2 is ON. This will produce $V_{OUT} \sim 0$ V, as shown in the Fig. (a).

2. When input is LOW, the gate of Q_1 (p-channel) is at a negative potential relative to its source while Q2 has Vgs = 0 V. Thus, is ON and Q_2 is OFF. This produces output voltage approximately + VDD, as shown in the Fig. (b).

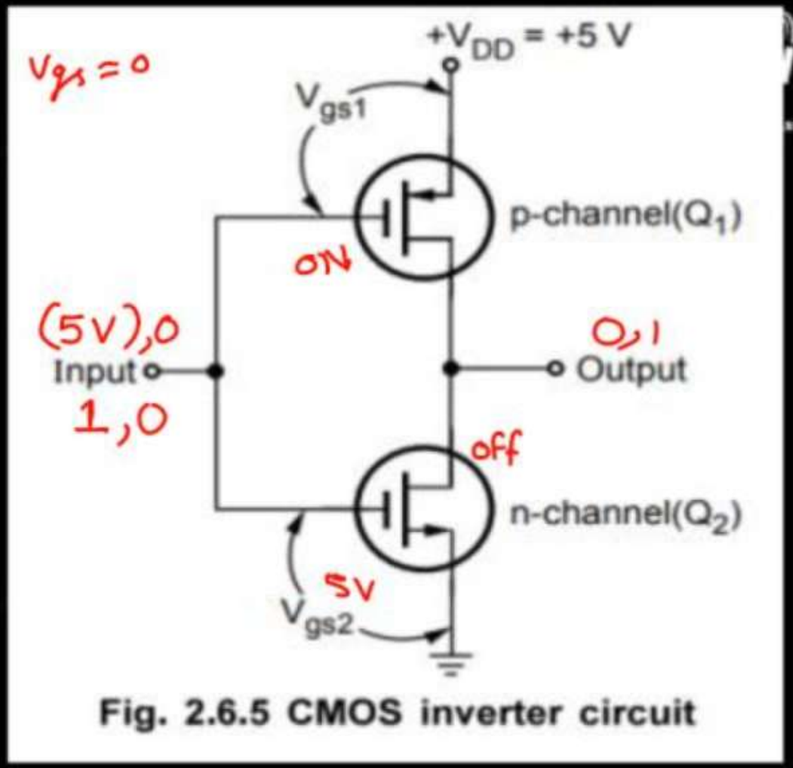
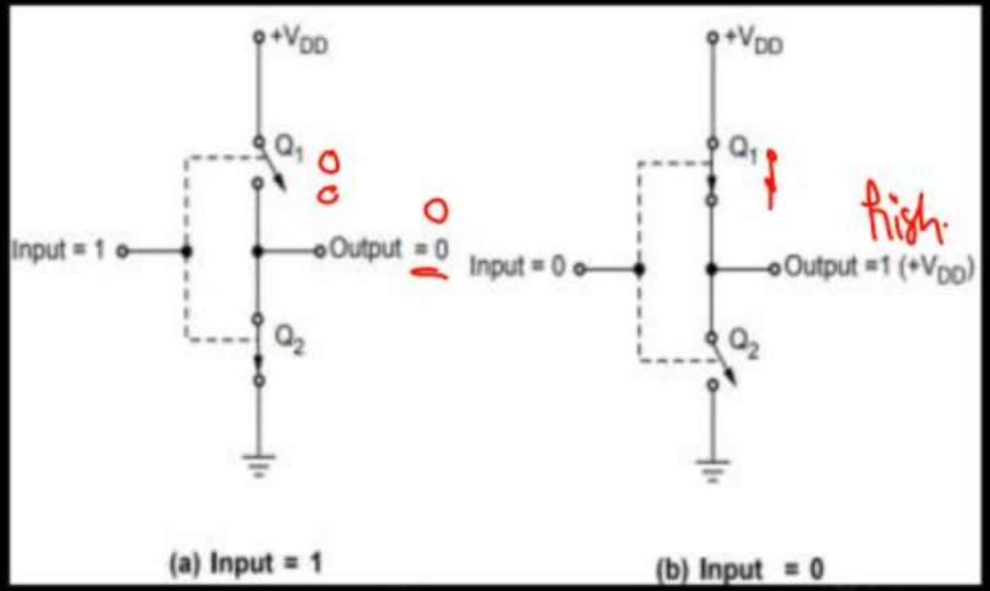


Fig. 2.6.5 CMOS inverter circuit



Gateway Classes

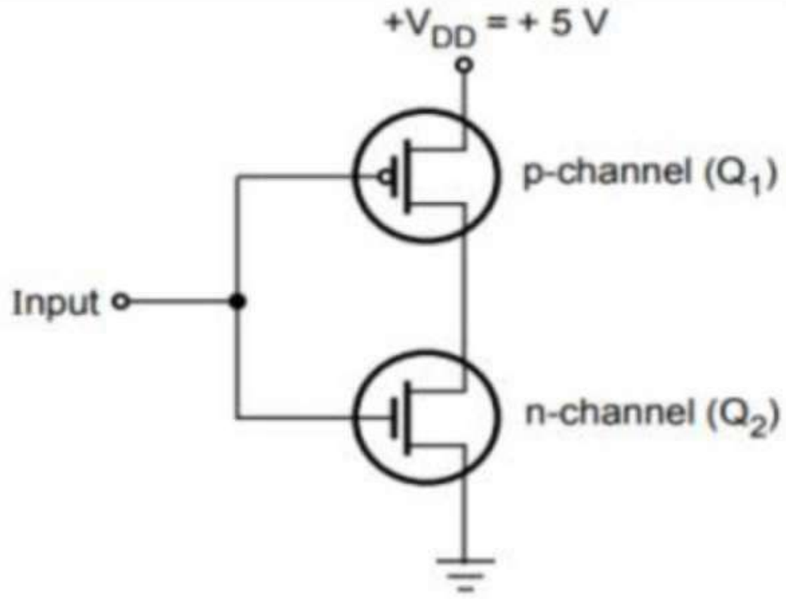
The operation of CMOS inverter circuit.

A	Q_1	Q_2	Output
0	ON	OFF	1
1	OFF	ON	0

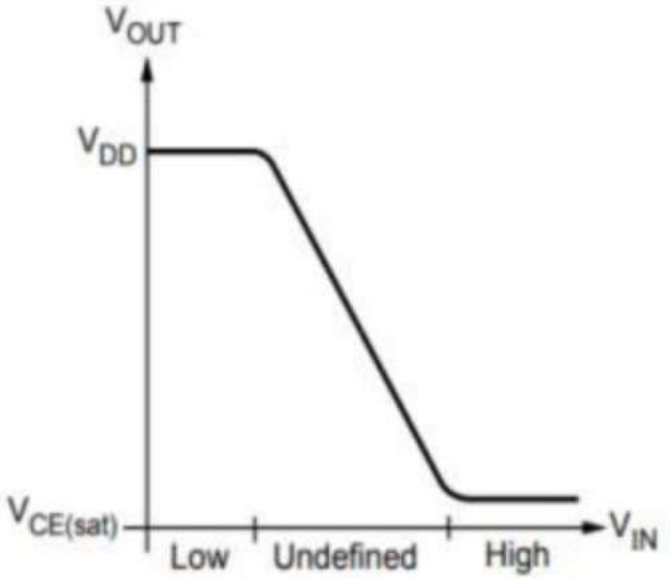
Table 2.6.4 Truth table of inverter

The Fig. shows, different symbols used for the p-channel and n-channel transistors to reflect their logical behaviour. The n-channel transistor (Q2) is switched 'ON' when a HIGH voltage is applied at the input. The p-channel transistor (Qi) has the opposite behaviour, it is switched ON when a LOW voltage is applied at the input. It is indicated by placing bubble in the symbol.

The Fig. shows the transfer characteristics of CMOS inverter.



The CMOS inverter

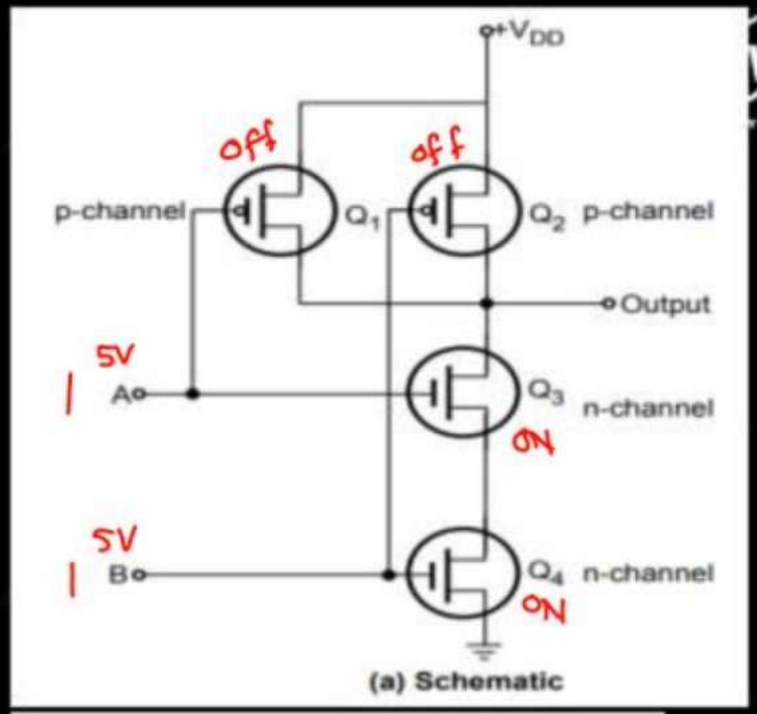


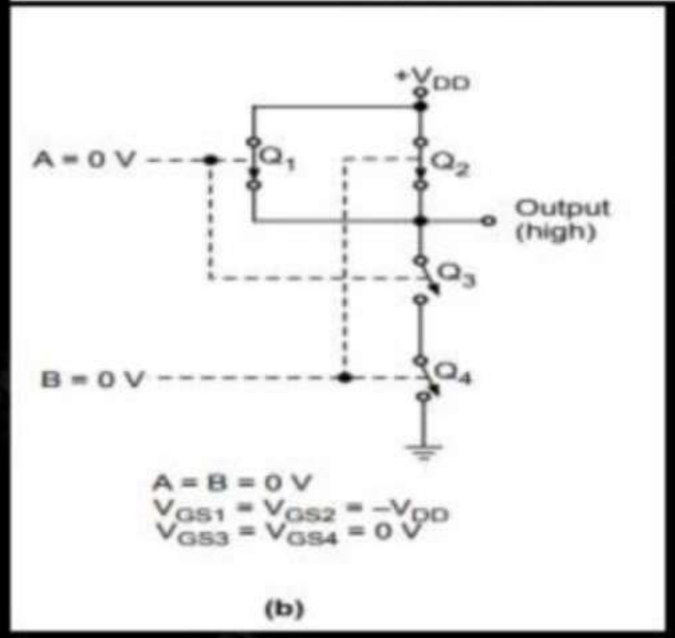
CMOS inverter transfer characteristics

Gateway Classes

COMS NAND Gate

- Fig. shows CMOS 2-input NAND gate. It consists of two p-channel MOSFETs, Q4 and Q2, connected in parallel and two n-channel MOSFETs, Q3 and Q4 connected in series.
- Fig.(a) shows the equivalent switching circuit when both inputs are low. Here, the gates of both p-channel MOSFETs are negative with respect to their sources, since the sources are connected to + VDD.
- Thus, Q1 and Q2 are both ON. Since the gate-to-source voltages of Q3 and Q4 (n-channel MOSFETs) are both 0 V, those MOSFETs are OFF.
- The output is therefore connected to +VDD (HIGH) through Q4 and Q2 and is disconnected from ground, as shown in the Fig. (b)

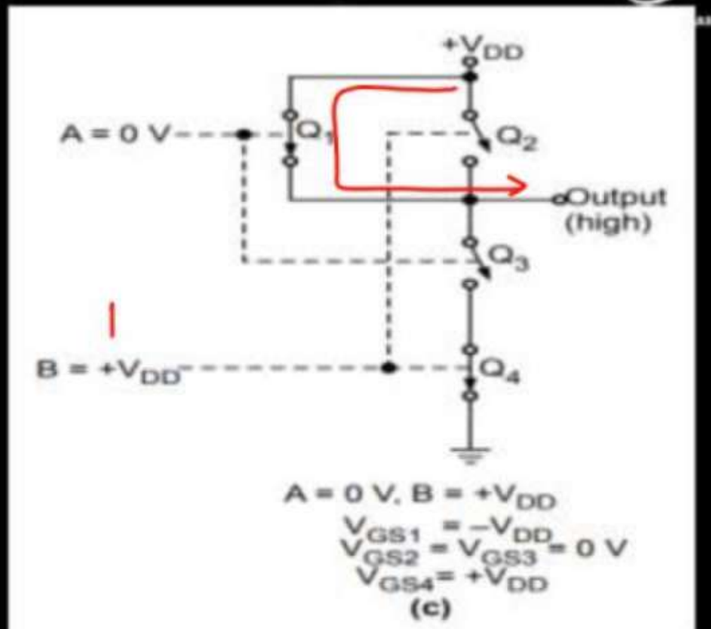




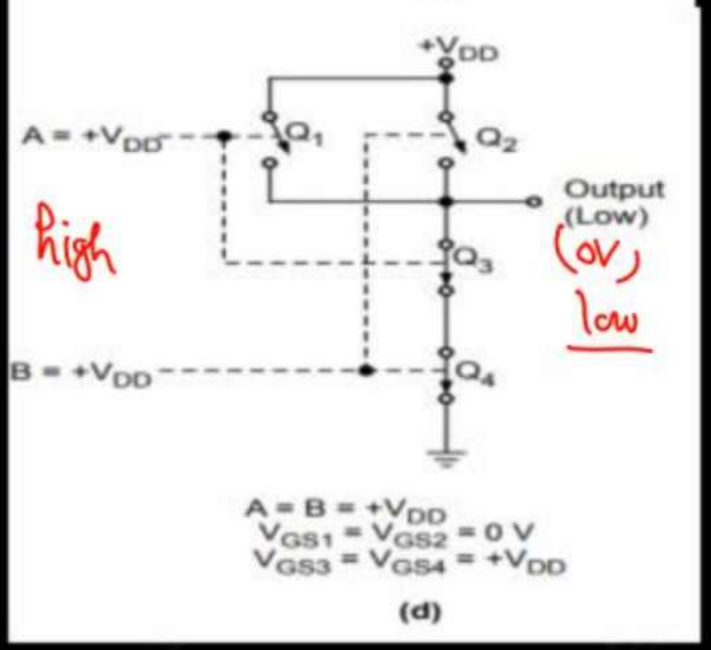
Gateway Classes

COMS NAND Gate

- Fig. (c) shows the equivalent switching circuit when A = 0 and B = +VDD. In this case, Q4 is on because VGSi= - VDD and Q4 is ON because VGg4 = +VDD.
- MOSFETs Q2 and Q3 are off because their gate-to-source voltages are 0 V. Since Q4 is ON and Q3 is OFF, the output is connected to +VDD and it is disconnected from ground.
- When A = +VDD and B = 0 V, the situation is similar (not shown); the output is connected to +VDD through Q2 and it is disconnected from ground because Q4 is OFF.
- Finally, when both inputs are high (A = B = +VDD), MOSFETs Q1 and Q2 are both OFF and Q3 and Q4 are both ON. Thus, the output is connected to the ground through Q3 and Q4 and it is disconnected from + VDD.



(c)



(d)

Gateway Classes

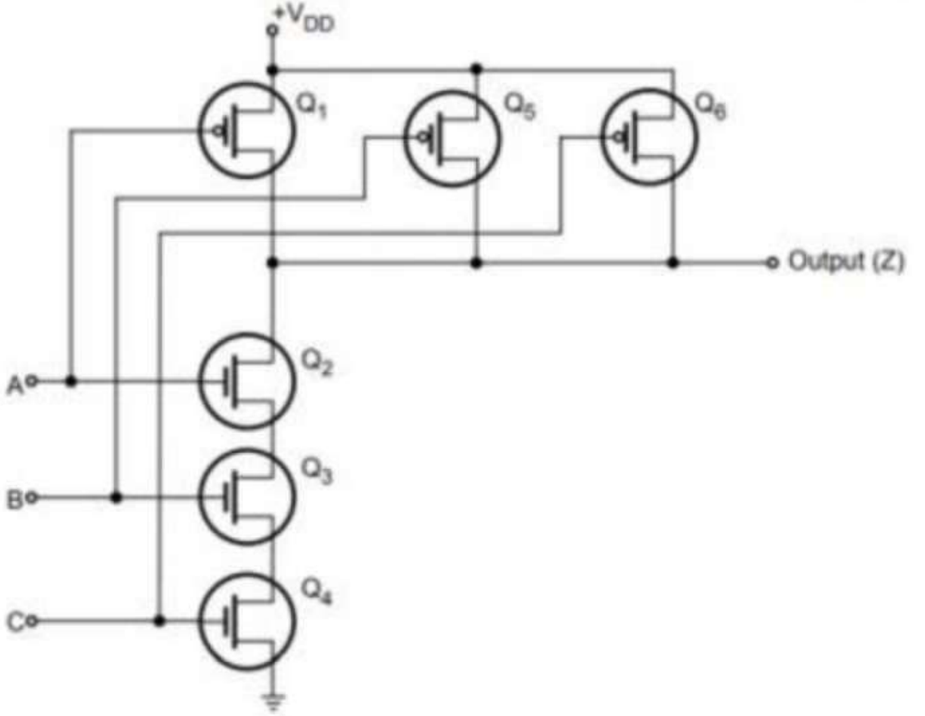
COMS NAND Gate

- The Table summarizes the operation of 2-input CMOS NAND gate.

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Table 2.6.5 Truth table of NAND gate

- Note : p-channel MOSFET is ON when its gate voltage is negative with respect to its source whereas n-channel MOSFET is ON when its gate voltage is positive with respect to its source
- The Fig. shows the circuit diagram, function table and logic symbol of CMOS 3-input NAND gate.



(a) Circuit diagram

A	B	C	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Z
0	0	0	ON	OFF	OFF	OFF	ON	ON	1
0	0	1	ON	OFF	OFF	ON	ON	OFF	1
0	1	0	ON	OFF	ON	OFF	OFF	ON	1
0	1	1	ON	OFF	ON	ON	OFF	OFF	1
1	0	0	OFF	ON	OFF	OFF	ON	ON	1
1	0	1	OFF	ON	OFF	ON	ON	OFF	1
1	1	0	OFF	ON	ON	OFF	OFF	ON	1
1	1	1	OFF	ON	ON	ON	OFF	OFF	0

(b) Function table

Gateway Classes

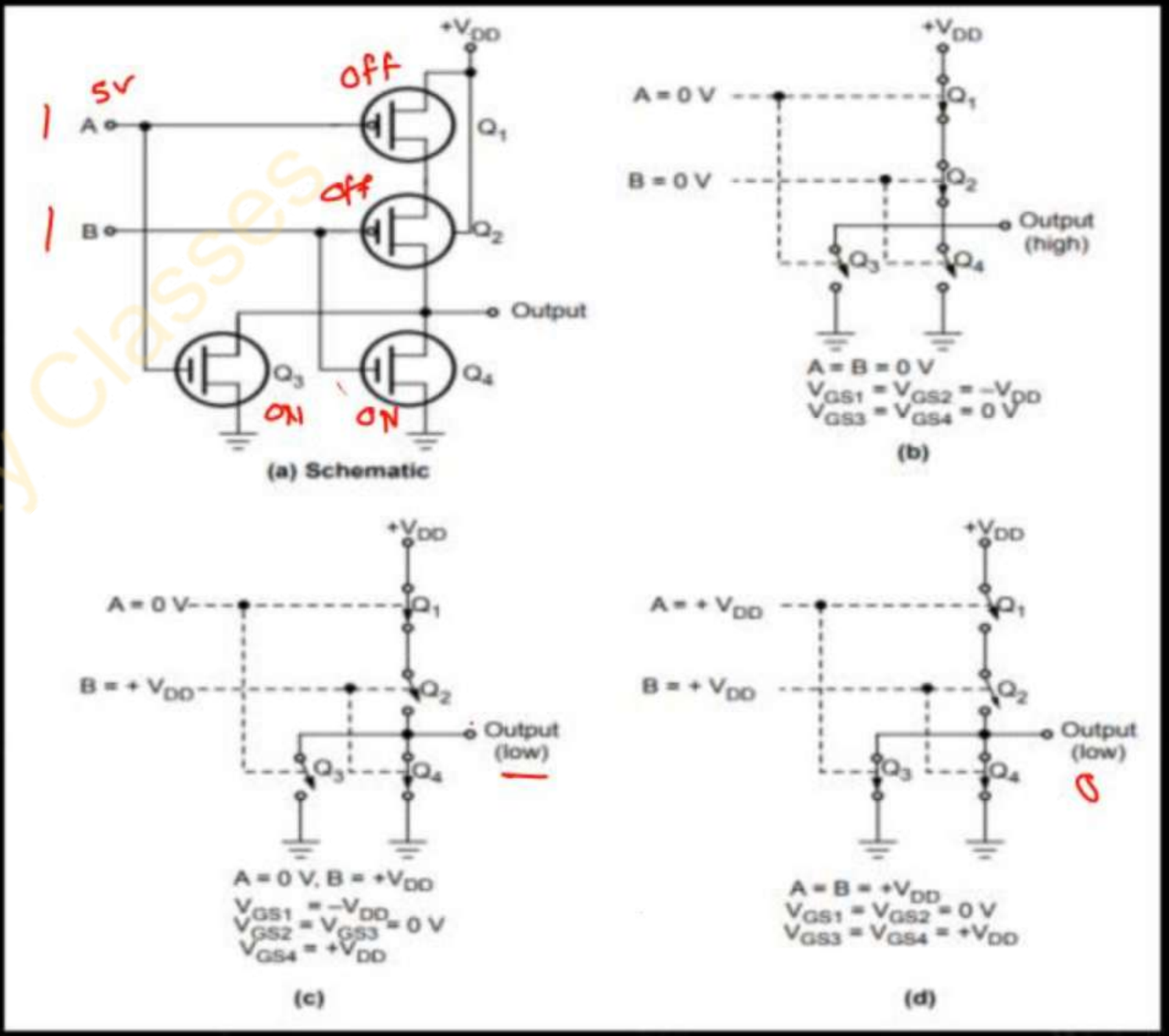
COMS NOR Gate

➢ shows 2-input CMOS NOR gate. Here, p-channel MOSFETs and Q2 are connected in series and n-channel MOSFETs Q3 and Q4 are connected in parallel.

Like NAND circuit, this circuit can be analyzed by realizing that a LOW at any input turns ON its corresponding p-channel MOSFET and turns OFF its corresponding n-channel MOSFET, and vice versa for a HIGH input. This is illustrated in Fig. 2.6.11. The Table 2.6.6 summarizes the operation of 2-input NOR gate.

A	B	Q_1	Q_2	Q_3	Q_4	Output
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

Table 2.6.6 Truth table for NOR gate



Gateway Classes

Advantages and Disadvantages of CMOS Family

Advantages

- 1. Consumes less power.
- 2. Can be operated at high voltages, resulting in improved noise immunity.
- 3. Fan-out is more.
- 4. Better noise margin.

Disadvantages

- 1. Susceptible to static charge.
- 2. Switching speed low.
- 3. Greater propagation delay

Gateway Classes

AKTU B.Tech II-Year

GATEWAY CLASSES

EC & EC Allied

DSD : Digital System Design

Unit-4 Lec-4

Gateway Classes

Today's target

- Interfacing of Logic families
- PYQ

Avinash Sir

AKTU : ***DIGITAL SYSTEM DESIGN (BEC-302)*** **Syllabus**

UNIT- 4

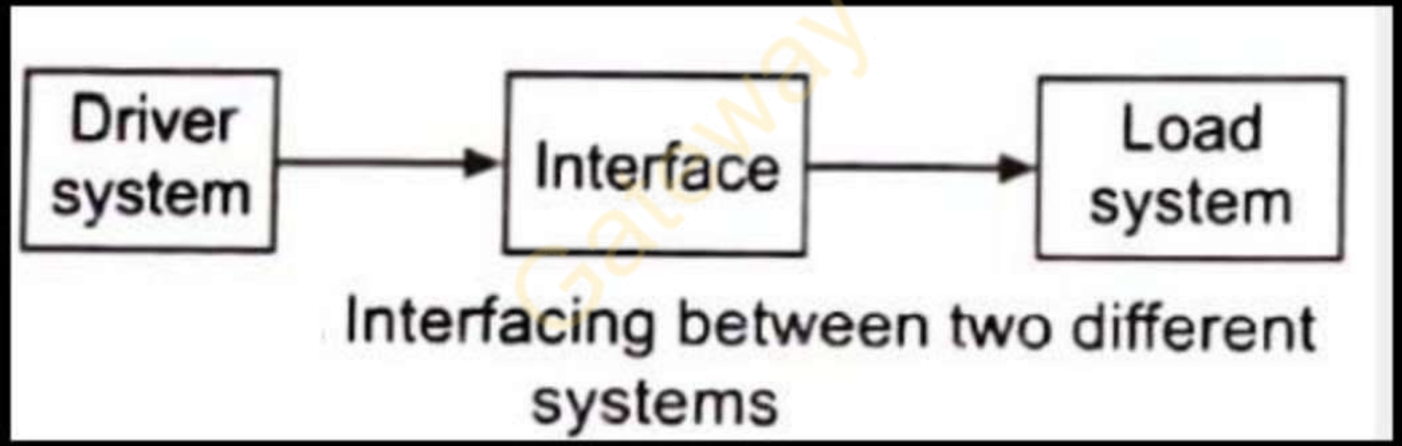
- Logic families and semiconductor memories: TTL NAND gate, specifications, noise margin, propagation delay, fan-in, fan-out, tristate TTL, ECL, CMOS families and their interfacing, memory elements, concept of programmable logic devices like FPGA, logic implementation using programmable devices.

Gateway Classes

Interface of logic Families

What is Interfacing?

- Interfacing = connecting the output of one logic family to the input of another.
- Needed when electrical characteristics differ (voltage levels, current levels).
- An interface circuit adjusts the signal so that the driver output becomes compatible with the load input.



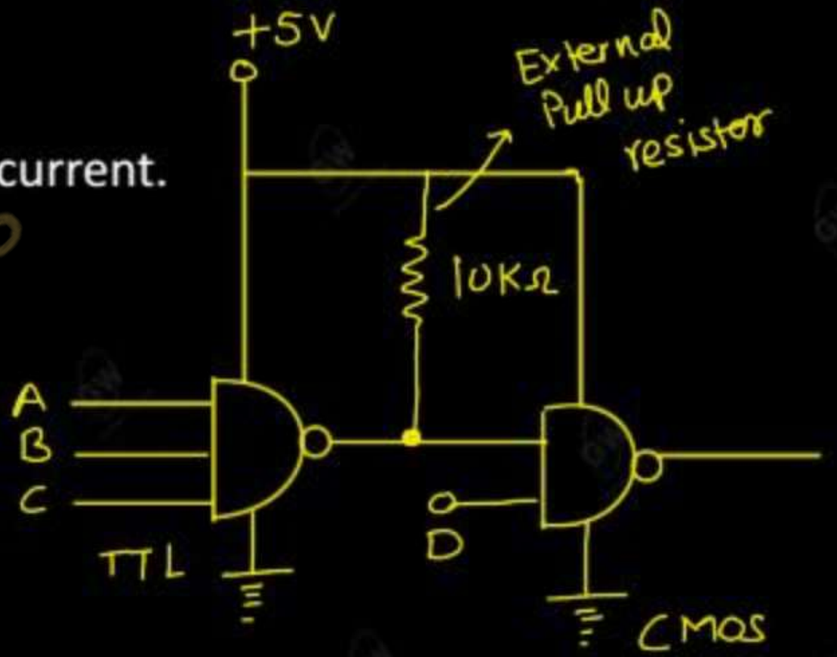
Interfacing between two different systems

Gateway Classes

TTL Driving CMOS

Basic Issue

- TTL and CMOS have different voltage levels.
- Current is not a problem because TTL output current > CMOS input current.
- Voltage mismatch is the major issue:
  - TTL VOH(min) is lower than CMOS VIH(min) requirement.
  - TTL HIGH output ≈ 2.4 V (min).
  - CMOS HIGH input requires ≥ 3.5 V (for 4000B).



Solution — Pull-up Resistor

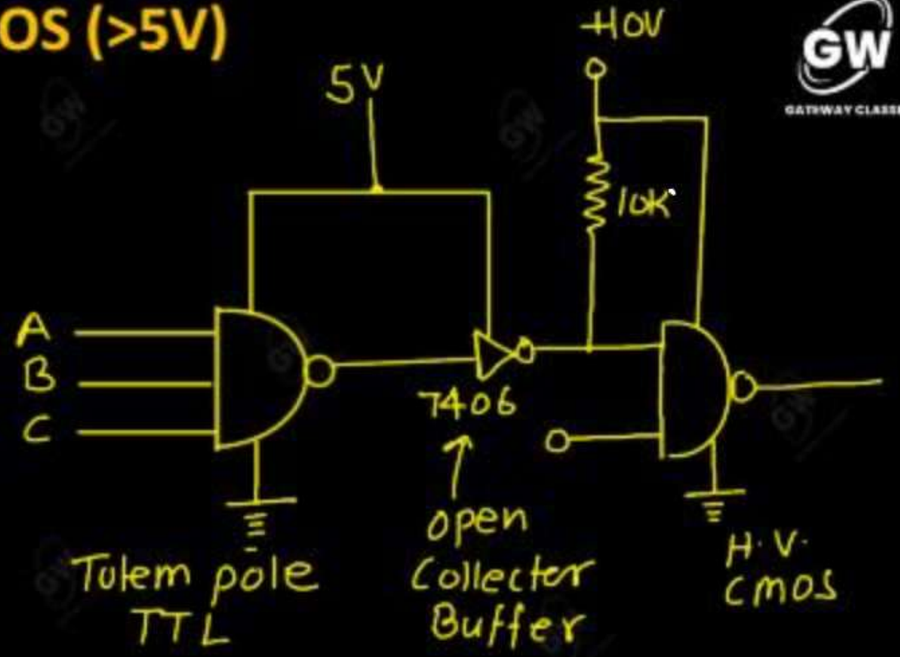
- A pull-up resistor (≈10 kΩ) is connected from TTL output to +5V.
- This raises TTL HIGH level to approx. 5 V → suitable for CMOS.
- Not required for:

  74HCT, 74ACT, These CMOS families accept TTL levels directly.

Gateway Classes

1.2. TTL Driving High-Voltage CMOS (>5V)

Problem:-High-voltage CMOS (e.g., VDD = 10–15V) requires HIGH input ≈ 7V or more. TTL cannot output >5V, so pull-up method cannot be used.

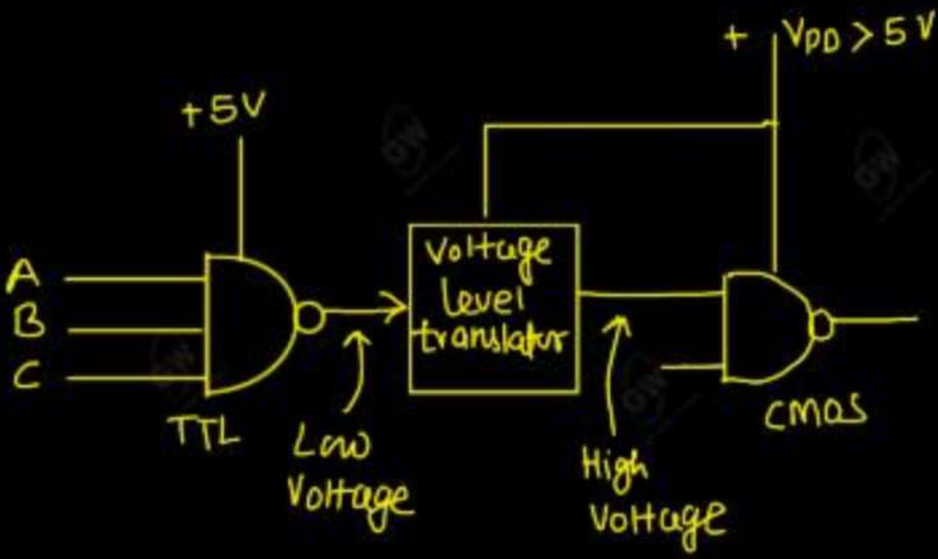


Solution —

- Open Collector Buffer (7406)Use 7406 (an inverting open-collector buffer) + pull-up resistor to high voltage.
- 7406 supports output up to 30V.
- Pull-up resistor raises the output to CMOS supply.

1.3 Interfacing Using Level Shifters

- A level shifter IC (e.g., 4504B) converts TTL 5V levels → CMOS higher voltage.
- Used when: Direct pull-up is not possible.
- Output sequencing must be clean. Voltage difference is large.



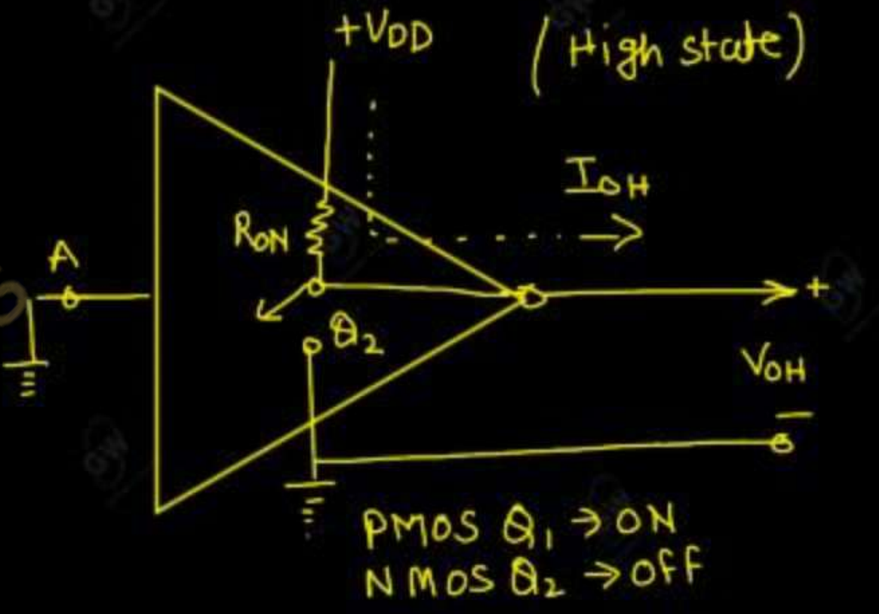
Gateway Classes

CMOS Driving TTL

To analyze, understand CMOS inverter outputs:

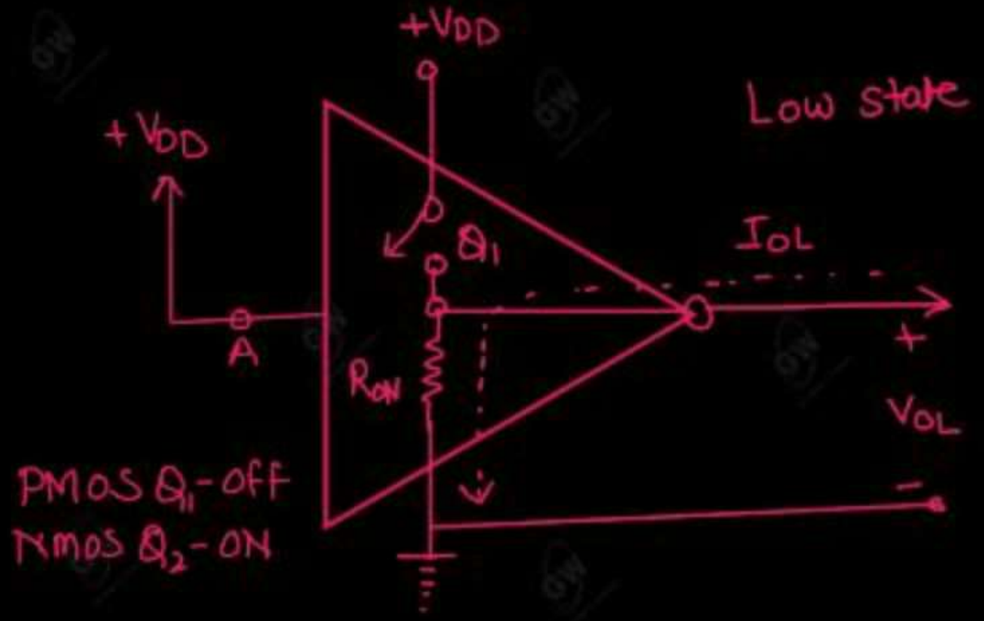
CMOS Output — HIGH State (equivalent circuit)

- PMOS ON → represented as RON (100 Ω – 1000 Ω).
- NMOS OFF → open switch.
- Acts like VDD source with series resistance RON.



CMOS Output — LOW State (equivalent circuit)

- PMOS OFF.
- NMOS ON → represented as RON to ground.
- Acts as low-resistance to ground.



CMOS driving TTL in HIGH State

- CMOS HIGH output (≈4.9–5V) > TTL VIH(min) (≈2V).
- CMOS I_{oH} can supply TTL input current easily.
- No interface needed.

Gateway Classes

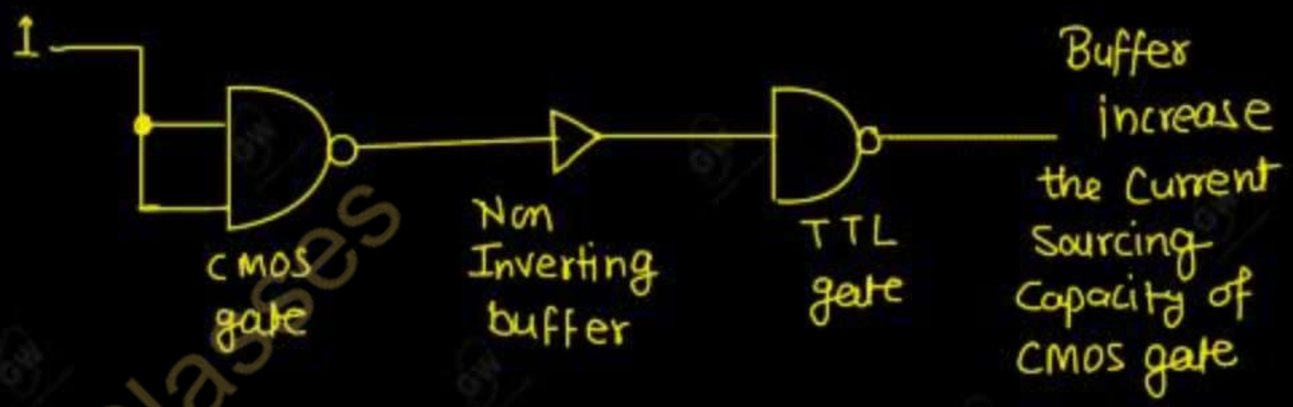
CMOS driving TTL in LOW State

Problem

- CMOS LOW output current IOL ≈ 0.4 mA.
- TTL input low current requires 1.6 mA.
- Thus, CMOS cannot sink enough current.

Solution

- Use a non-inverting buffer between CMOS and TTL.
- Buffer increases the current sinking capacity.



Gateway Classes

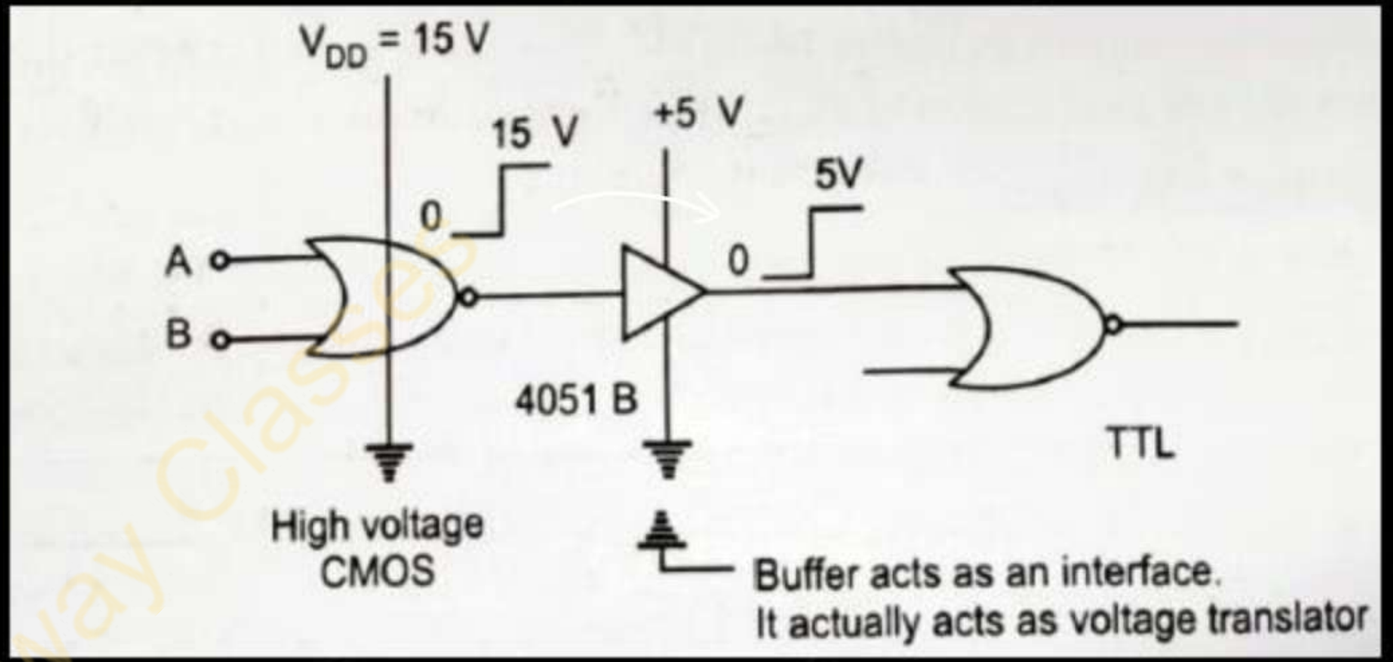
High-Voltage CMOS Driving TTL

Problem

- HV CMOS outputs ≈ 10–15V.
- TTL max input voltage allowed = 7V.
- Applying 15V would damage TTL.

Solution

- Use 4051B buffer (operates at +5V).
- Converts 15V CMOS HIGH → 5V TTL HIGH.
- Works as a voltage level translator.



Gateway Classes

Interfacing CMOS/TTL with ECL

Why Needed?

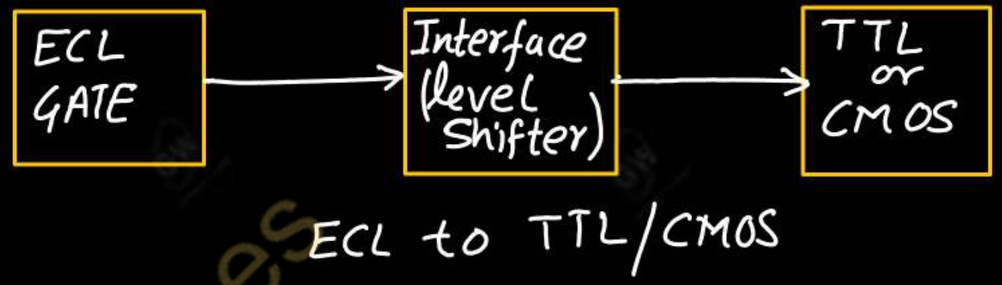
ECL has very different voltage levels:

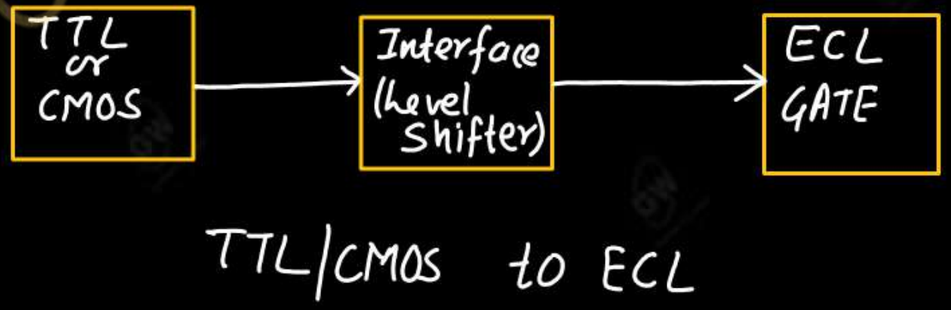
Operates around –5.2V

Logic HIGH ≈ –0.9V

Logic LOW ≈ –1.7V

TTL/CMOS cannot directly interface.





Solution

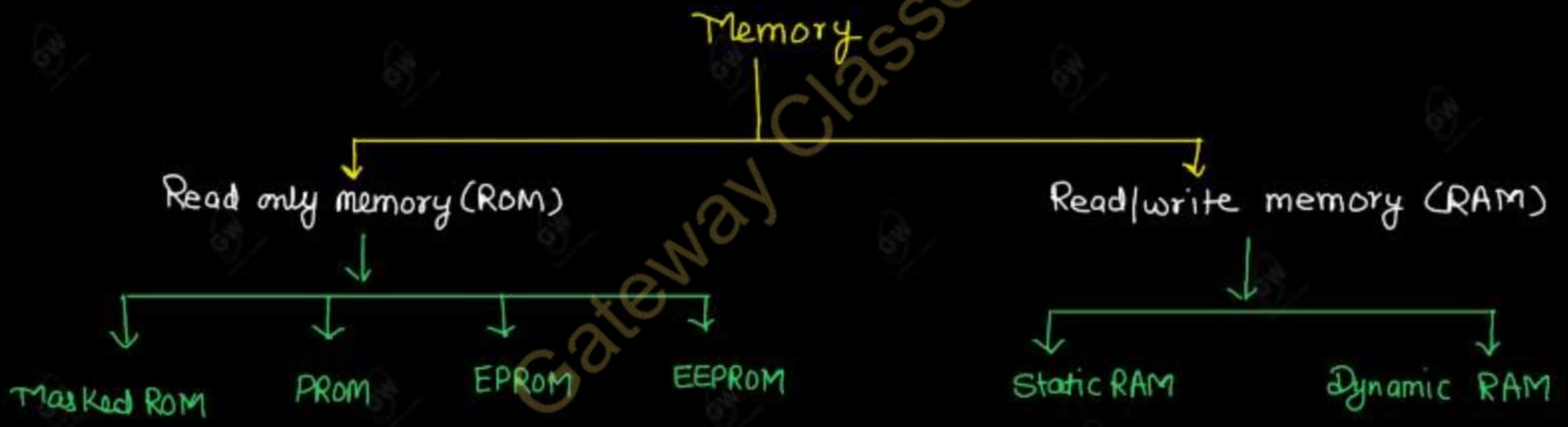
- Use voltage translators (in ECL families):
- TTL/CMOS → ECL converter
- ECL → TTL/CMOS converter

These circuits shift voltage levels safely.

Gateway Classes

Memory?

In the field of digital electronics, the memory is a device that is used to store data and instruction in the digital systems like computers and other microprocessor-based systems.



Gateway Classes

Types of ROMs

ROM : Read only memory: Its non volatile memory, ié, the information stored in it, is not lost even if the power supply goes off. It's used for the permanent storage of information.

The following types of ROMs an listed below :

(i) **PROM :** It's programmable ROM. Its contents are decided by the user. The user can store permanent programs, data etc in a PROM.

(ii) **EPROM :** An EPROM is an erasable PROM. The stored data in EPROM's can be erased by exposing it to UV light for about 20 min. It's not easy to erase it because the EPROM IC has to be removed from the computer and exposed to UV light.

(iii) **EEPROM (Electrically Erasable PROM) :** The chip can be erased & reprogrammed on the board easily byte by byte. It can be erased with in a few milliseconds.

Gateway Classes

COMBINATIONAL PLDs

Basic configuration of three PLDs are

1. PROM
2. programmable array logic (PAL)
3. Programmable logic array (PLA)

(a) Programmable read-only memory (PROM)

(b) Programmable array logic (PAL)

(c) Programmable logay aray (PLA)

Gateway Classes

COMBINATIONAL PLDs

A Programmable Logic Device (PLD) is an integrated circuit that can be configured or "programmed" by the user to implement specific logic functions .

Basic Structure: PLDs are essentially a combination of AND gates and OR gates .

Programmability: The connections within the AND array and OR array can be programmed (made or broken) by the user according to the required function

Categories of PLDs (Based on Programmability)

PLA (Programmable Logic Array): Both the AND array and the OR array are programmable.

PAL (Programmable Array Logic): The AND array is programmable, but the OR array is fixed (hardwired)

Gateway Classes

$(A + AB)$
$A(1+B) = A$

1. Logic Function Implementation using PLA

The primary goal is to implement a logic function using the PLA architecture .

Requirement: Minimized Boolean Expression To implement any function using a PLA. If the expression is not minimized (e.g., A + AB), it must be minimized first (e.g., to A) before implementation .

If the question provides minterms or a truth table, the function must first be calculated and minimized using a K-Map.

Calculating Required Gates (Size of the PLA)For implementing multiple output functions using a single PLA:

Number of OR Gates: This is equal to the Number of Output Functions .Example: If you have two functions (F1 and F2), you need two OR gates.

Number of AND Gates: This is equal to the total number of unique product terms found by combining all the functions.

Crucial Rule: Repeated product terms are NOT considered again (they are counted only once) .

Gateway Classes

Ex-1 A Combinational Circuit is defined by function

$F_1 = \Sigma m(3,5,7)$, $f_2 = \Sigma m(4,5,7)$

Implement the Circuit with PLA

Soln

F_1

A \ BC	00	01	11	10
0	0	1	1 (3)	2
1	1 (4)	1 (5)	1 (7)	6

$F_1 = \underline{BC} + \underline{AC}$

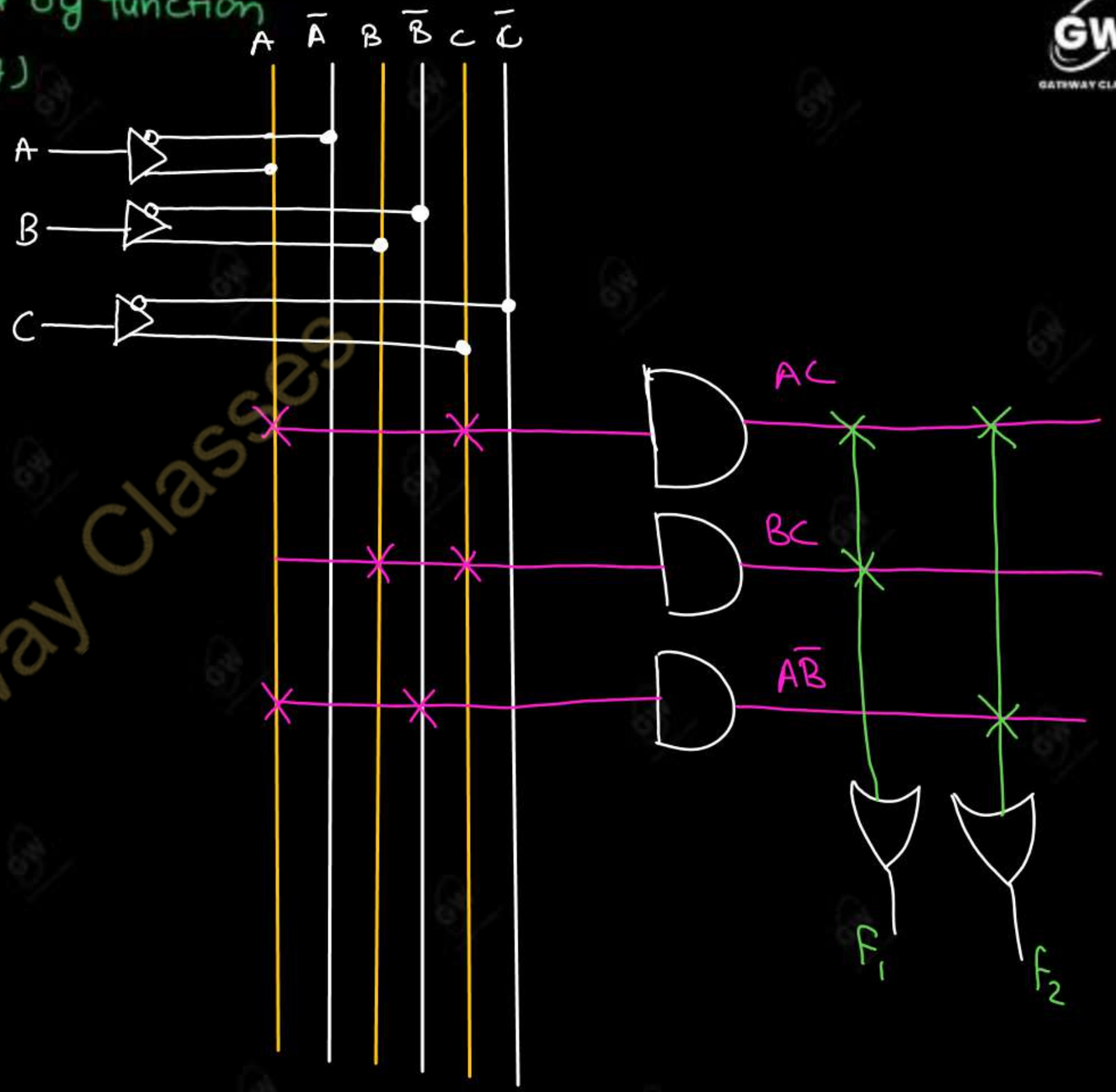
F_2

A \ BC	00	01	11	10
0	0	1	2	3
1	1 (4)	1 (5)	1 (7)	6

$F_2 = \underline{A\bar{B}} + \underline{AC}$

No. of OR GATE = No. of function = 02

No. of AND GATE = No. of unique Product term = 03

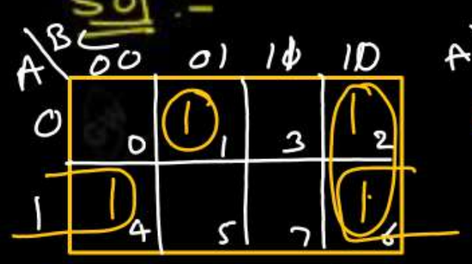


Gateway Classes

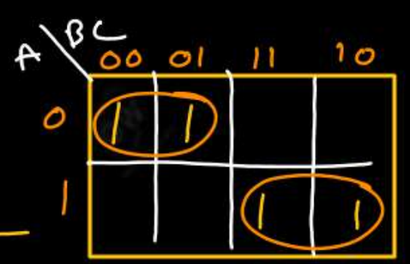
Ex-2 Implement the following function using PLA

$F_1(A,B,C) = \Sigma m(1,2,4,6)$, $F_2(A,B,C) = \Sigma m(0,1,6,7)$, $F_3(A,B,C) = \Sigma m(2,6)$

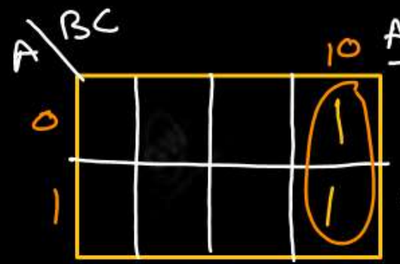
Sol :-



$F_1 = B\bar{C} + \bar{A}\bar{B}C + A\bar{C}$



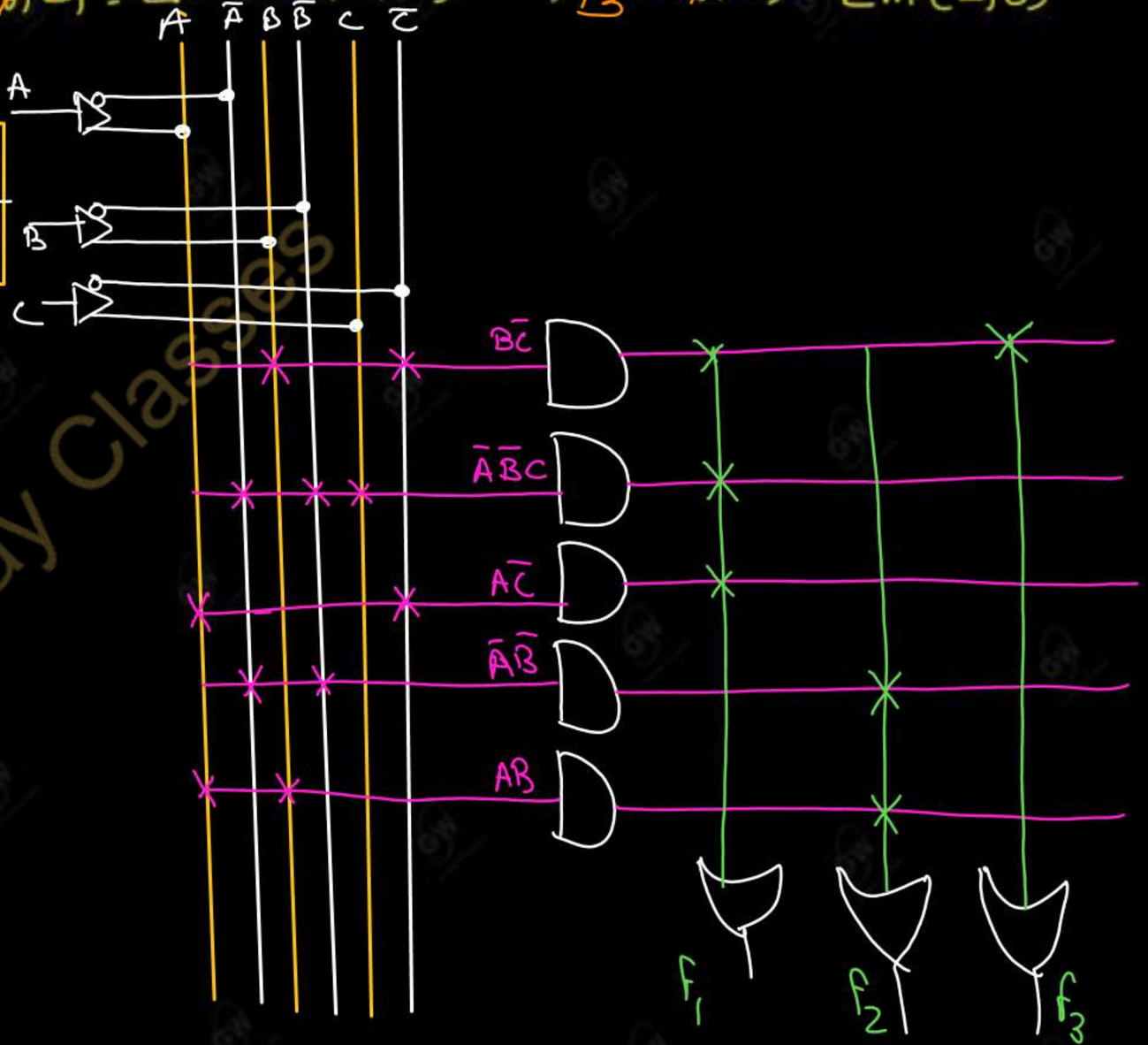
$f_2 = \bar{A}\bar{B} + AB$



$f_3 = B\bar{C}$

No. of OR GATE = 3 function = 3

No of AND GATE = 5



Gateway Classes

2. PAL (Programmable Array Logic)

PAL is another type of Programmable Logic Device (PLD).

Key Difference from PLA: In PAL, the AND array is programmable (like in PLA), but the OR logic (array) is fixed (hardwired). The fixed OR logic is the defining characteristic of the PAL structure.

Sizing the PAL (Calculating Required Gates)

To implement a function using PAL, the calculation for the number of gates reflects the fixed nature of the OR array.

Number of OR Gates: Equal to the Number of Output Functions (same as PLA).

Number of AND Gates: Calculated by finding the Maximum number of product terms in any single function, then multiplying by the Total number of functions.

Total AND Gates = Max Product Terms per Function x Number of Functions

Contrast with PLA: Unlike PLA, there is no concept of not considering repeated product terms. In PAL, an AND gate combination is fixed for each output function based on the maximum required.

Gateway Classes

Q: Implement the following Boolean function using suitable PAL

$W(A,B,C,D) = \Sigma m(1,3,4,6,9,11,12,14)$

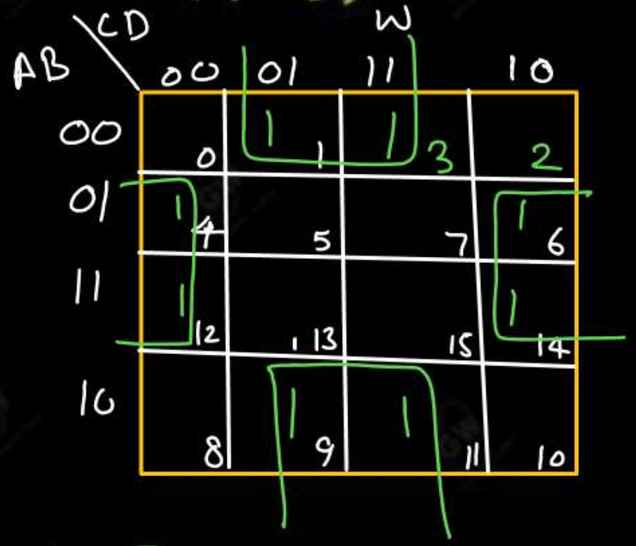
$x(A,B,C,D) = \Sigma m(1,3,4,6,9,11,12,14,15)$

$y(A,B,C,D) = \Sigma m(0,2,4,6,8,12)$

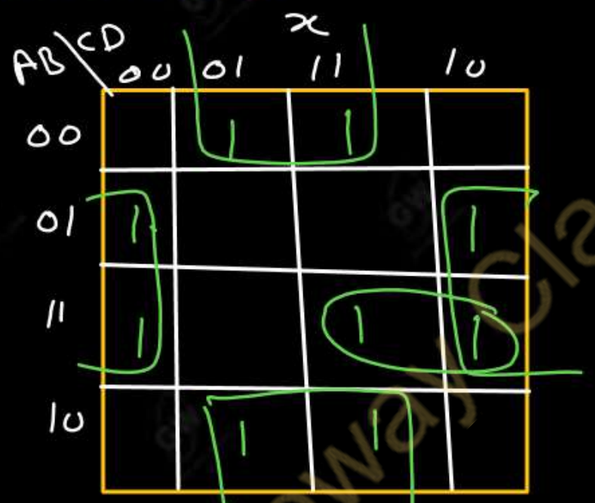
$Z(A,B,C,D) = \Sigma m(2,3,8,9,12,13)$

No. of OR GATE = No. of fun = 4

No. of AND GATE = 2 × 4 = 8

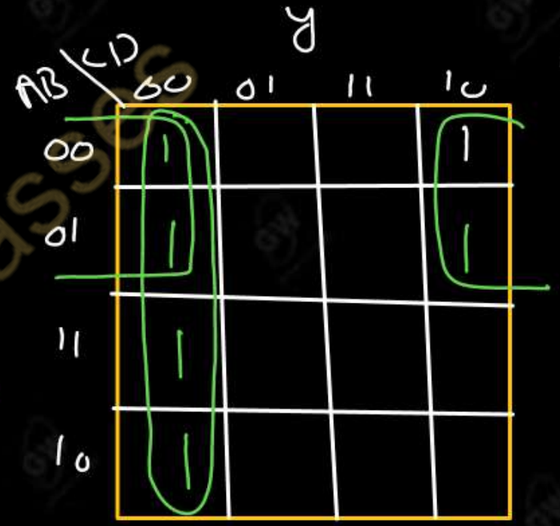


$W = \bar{B}D + B\bar{D}$

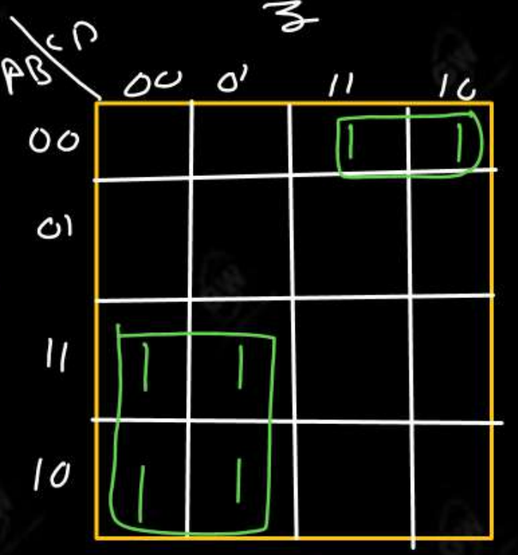


$x = B\bar{D} + \bar{B}D + ABC$

$x = W + ABC$

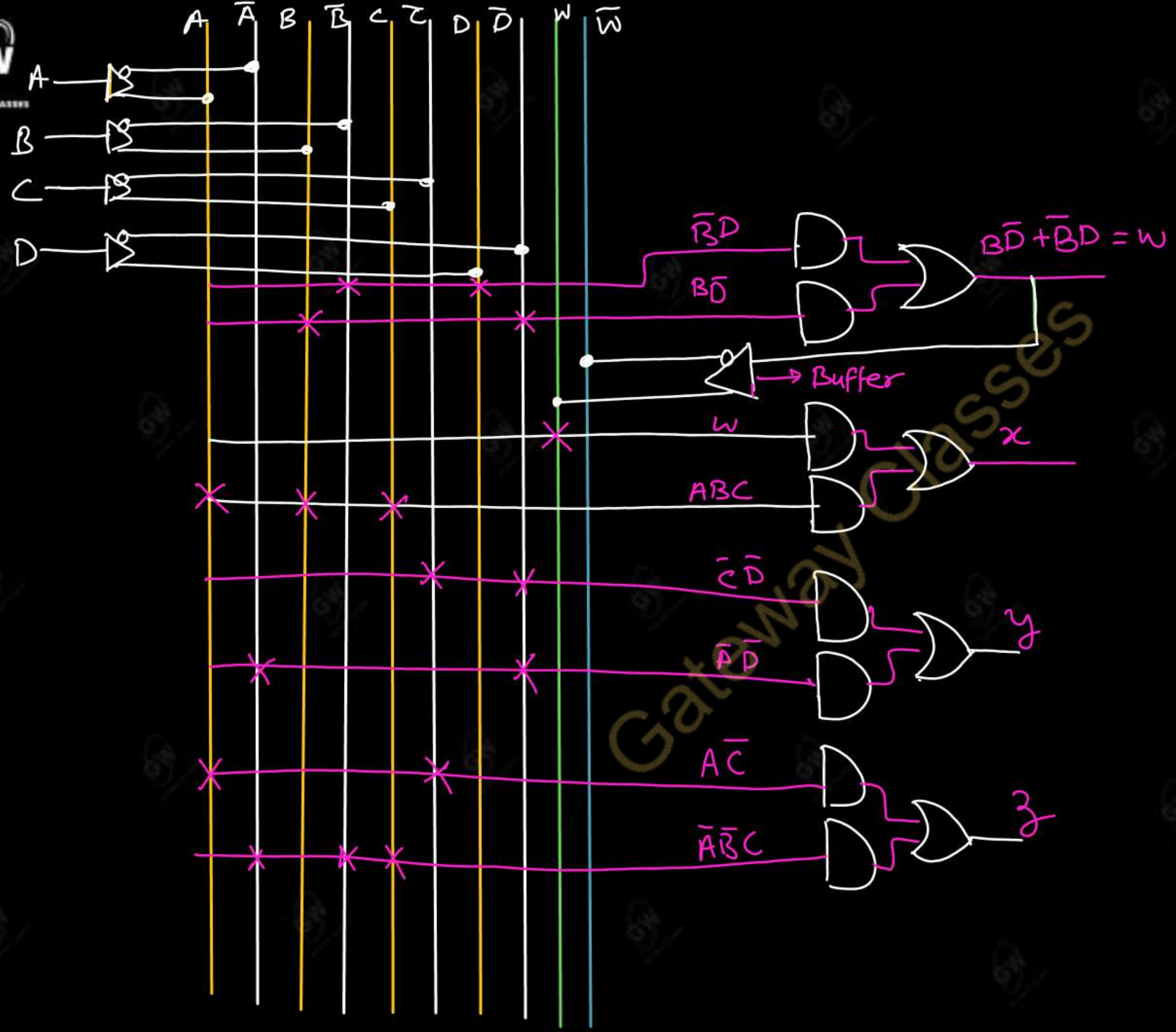


$y = \bar{C}\bar{D} + \bar{A}\bar{D}$



$z = A\bar{C} + \bar{A}\bar{B}C$

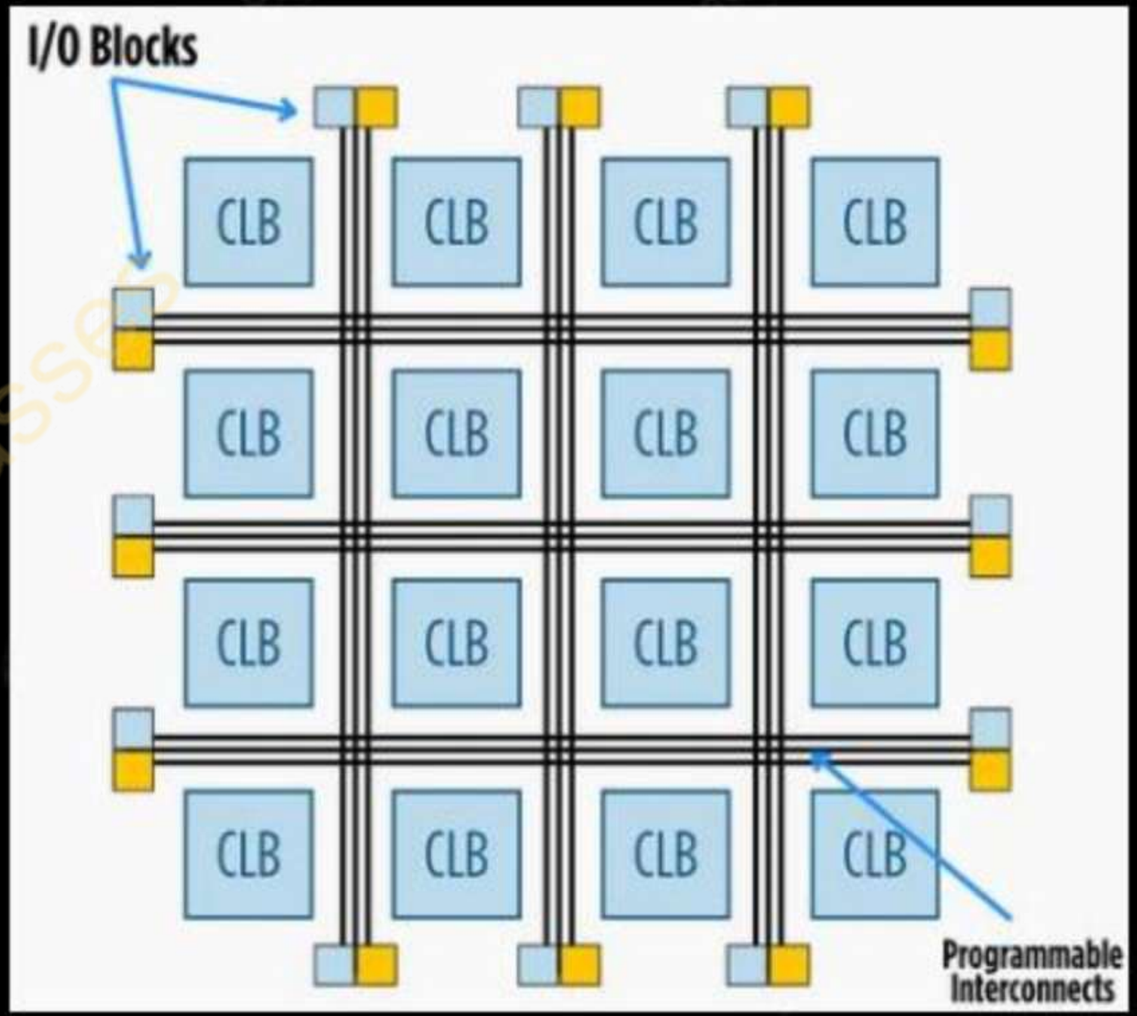
Gatewayclasses



GW GATEWAY CLASSES
GW GATEWAY CLASSES
Gateway Classes

Field Programmable Gate Array (FPGA)

- An FPGA (Field Programmable Gate Array) is a type of integrated circuit in digital electronics that can be programmed and reprogrammed after manufacturing to perform custom digital logic functions.
- They are built with a grid of configurable logic blocks (CLBs) and programmable interconnects, allowing designers to create custom circuits for tasks like signal processing, embedded systems, and high-performance computing.
- The configuration of the FPGA architecture is generally specified using a language, i.e., HDL (Hardware Description Language), which is similar to the one used for an ASIC (Application Specific Integrated Circuit).



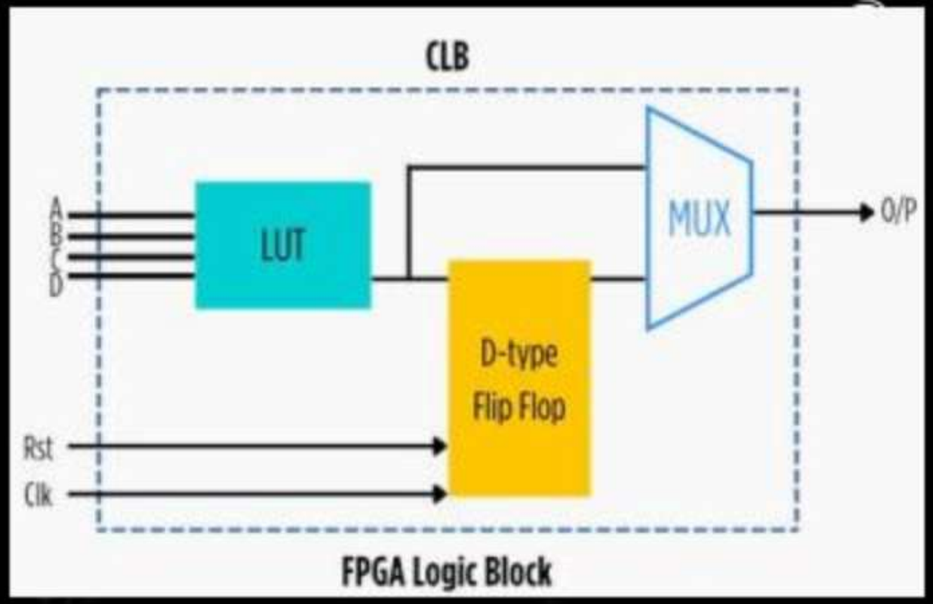
Gateway Classes

FPGA Architecture

- **Configurable Logic Blocks (CLBs):** The core of FPGA functionality, these blocks contain logic gates and a small amount of memory that can be programmed to perform various logical functions. They are the building blocks for creating more complex digital circuits.

  LUT (Look Up Table) implements the combinational logical functions; the MUX (Multiplexer) is used for selection logic, and DFF (D type flip flop) stores the output of the LUT.

- **Programmable Interconnects:** A network of programmable wiring that connects the logic blocks. These interconnects can be configured to route signals between different logic blocks, allowing the creation of complex digital circuits by defining how data flows through the FPGA.



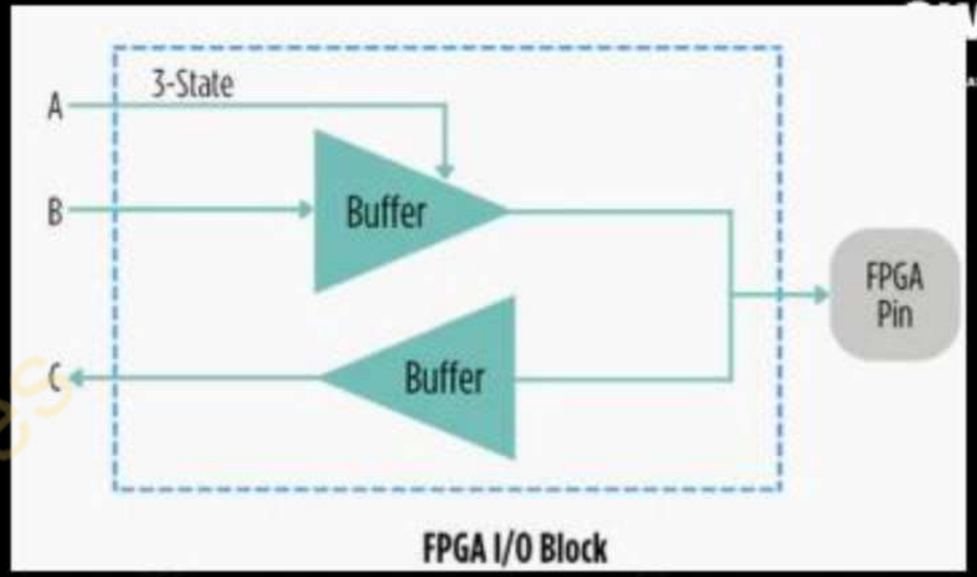
FPGA Logic Block

FPGA Interconnect

Gateway Classes

FPGA Architecture

I/O Blocks (Input/Output Blocks): Located next to every physical input or output pin, these blocks connect the internal logic of the FPGA to the external environment. They can be programmed to act as inputs, outputs or tri-states, enabling the FPGA to communicate with external devices and systems.



FPGA I/O Block

Advantages of FPGAs

- Flexibility: FPGAs can be reprogrammed to perform different tasks or update the functionality of a device after it has been deployed. This allows for modifications and improvements without needing to redesign the hardware.
- Rapid Prototyping: Designers can quickly implement and test their designs on FPGAs, making them ideal for prototyping and iterative development processes.
- Lower Initial Costs: For low to medium-volume productions, FPGAs generally have lower upfront costs compared to developing an ASIC, as there are no expensive fabrication costs involved.

Gateway Classes

Application of FPGA

- Telecommunications: FPGAs are essential for signal processing and updating network protocols without replacing hardware.
- Data Centers: Accelerate data processing, encryption, and network management, enhancing server efficiency.
- Aerospace and Defense: FPGAs provide reliability in harsh environments, handling radar, communications, and encryption.
- Consumer Electronics: Utilized for processing in cameras, TVs, and home systems, improving digital experiences.
- Industrial Control: Streamline control systems, automation, and machine vision, facilitating real-time processing.
- Medical & Scientific Instruments: Essential in imaging equipment, FPGAs process complex algorithms quickly, ensuring rapid diagnostics. Support research with precision and speed in data acquisition and analysis.
- Artificial Intelligence and Machine Learning: Accelerate AI/ML training and inference, supporting rapid development and deployment.

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